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Power Supply Noise Management: Techniques for Estimation, Detection, and Reduction

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Power Supply Noise Management: Techniques for Estimation, Detection, and Reduction

by

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DISSERTATION

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Dedicate to my family, who supports me with endless love

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At the end, I would like to thank my wife, Ming-Chan Wu. She accompanied and supported me through these years when I was alone in this foreign country. She even changed her life plan and applied to the graduate school in UT. I feel so lucky to have a soul mate like her in my life, and I really appreciate her efforts to support me in pursuing my dream.

I used to think that finishing this degree would be a destination of this journey. However, now I realize that it is just a check point instead of a destination. I still do not know what kind of challenges are waiting for me in the future. However, I think this is the fun part, and I cannot wait to continue this amazing journey.

Power Supply Noise Management: Techniques for Estimation, Detection, and Reduction

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Power supply noise has become a critical issue for low power and high performance circuit design in recent years. The rapid scaling of the CMOS process has pushed the limit further and further in building low-cost and increasingly complex digital VLSI systems. Continued technology scaling has contributed to significant improvements in performance, increases in transistor density, and reductions in power consumption. However, smaller feature sizes, higher operation frequencies, and supply voltage reduction make current and future VLSI systems more vulnerable to power supply noise. Therefore, there is a strong demand for strategies to prevent problems caused by power supply noise.

Design challenges exist in different design phases to reduce power supply noise. In terms of physical design, careful power distribution design is required, since it directly determines the quality of power stability and the timing integrity. In addition, power management, such as switching mode of the power gating technique, is another major challenge during the circuit design phase. A bad power

gating switching strategy may draw an excessive rush current and slow down other active circuitry. After the circuit is implemented, another critical design challenge is to estimate power supply noise. Designers need to be aware of the voltage drop in order to enhance the power distribution network without wasting unnecessary design resources. However, estimating power supply noise is usually difficult, especially finding the circuit activity which induces the maximum supply noise. Blind search may be very time consuming and not effective. At post-silicon test, detecting power supply noise within a chip is also challenging. The visibility of supply noise is low since there is no trivial method to measure it. However, the supply noise measurement result on silicon is critical to debug and to characterize the chip.

This dissertation focuses on novel circuit designs and design methodologies to prevent problems resulted from power supply noise in different design phases. First, a supply noise estimation methodology is developed. This methodology systematically searches the circuit activity inducing the maximum voltage drop. Meanwhile, once the circuit activity is found, it is validated through instruction execution. Therefore, the estimated voltage drop is a realistic estimation close to the real phenomenon. Simulation results show that this technique is able to find the circuit activity more efficiently and effectively compared to random simulation.

Second, two on-chip power supply noise detectors are designed to improve the visibility of voltage drop during test phase. The first detector facilitates insertion of numerous detectors when there is a need for additional test points, such as a fine-grained power gating design or a circuit with multiple power domains. It focuses on minimizing the area consumption of the existing detector. This detector

significantly reduces the area consumption compared to the conventional approach without losing accuracy due to the area minimization. The major goal of designing the second on-chip detector is to achieve self-calibration under process and temperature variations. Simulation and silicon measurement results demonstrate the capability of self-calibration regardless these variations.

Lastly, a robust power gating reactivation technique is designed. This reactivation scheme utilizes the on-chip detector presented in this dissertation to monitor power supply noise in real time. It takes a dynamic approach to control the wakeup sequence according to the ambient voltage level. Simulation results demonstrate the ability to prevent the excessive voltage drop while the ambient active circuitry induces a high voltage drop during the wakeup phase. As a result, the fixed design resource, which is used to prevent the voltage emergency, can potentially be reduced by utilizing the dynamic reactivation scheme.

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Chapter 1

Introduction

1.1 Power supply noise

Power supply noise indicates a non-ideal VDD on the local power-ground rails. It results from the impedance ($Z = R + j\omega L$) of the power supply network and the current that flows through the power supply network [1]. A lumped RLC model of power distribution including the voltage regulator module, mother board, package, and die is illustrated in Figure 1.1 [2]. Figure 1.2 [3] shows a typical waveform of power supply noise. Power supply noise can be classified into three categories, IR drop, Ldi/dt noise, and RLC resonance [4][5][6]. The IR drop usually results from on-chip power distribution, while Ldi/dt noise results from the package or the board inductance. The package inductance and the on-chip/on-board capacitor form a LC network and cause voltage resonance. Power supply noise can exist in both power and ground network. There is supply noise for power (ΔVDD) and supply noise for ground (ΔVSS) respectively. To simply the notation, people usually use effective VDD ($VDD_{actual} - VSS_{actual}$) to describe the effective supply noise ($\Delta VDD + \Delta VSS$). The supply noise in the rest of this dissertation indicates the effective supply noise.

Power supply noise can be either undershoot noise ($VDD < VDD_{ideal}$) or

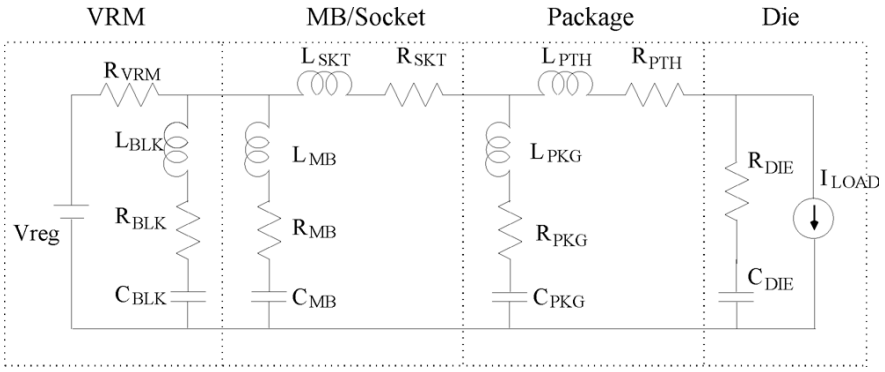


Figure 1.1: A lumped RLC model of voltage regulator module, mother board, package, and die

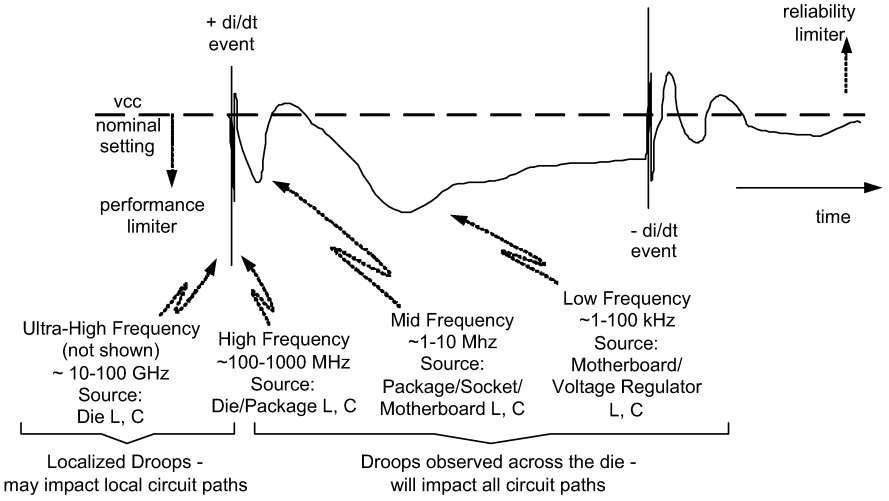


Figure 1.2: Microprocessor Vdd fluctuations caused by interaction of parasitics with changes in current demand

overshoot noise ($VDD > VDD_{ideal}$). Transient undershoot noise can slow down a circuit and cause timing failures, while overshoot noise can cause reliability and power consumption problems. Both types of noise may cause jitter within the PLL/DLL and the clock distribution network [7] [8]. Previous research [9] reveals that power supply noise is an important factor affecting signal integrity and causing timing uncertainty in modern technologies as shown in Table 1.1.

Power supply noise has become even more critical as technology advances. The rapid scaling of the CMOS process has been a prominent reason for its wide use in building low-cost and increasingly complex digital VLSI systems. Continued technology scaling has contributed to significant improvements in performance, increases in transistor density, and reductions in power consumption. However, smaller feature sizes, higher operation frequencies, and supply voltage reduction make current and future VLSI systems more vulnerable to power supply noise [9][10][11]. Without a doubt, there is a strong demand for strategies to prevent problems caused by power supply noise.

1.2 Power supply noise challenges in different design phases

There are many design challenges in different design phases which must avoid power supply noise problems. These challenges can be illustrated in Figure 1.3 and are described more specifically in the following sections.

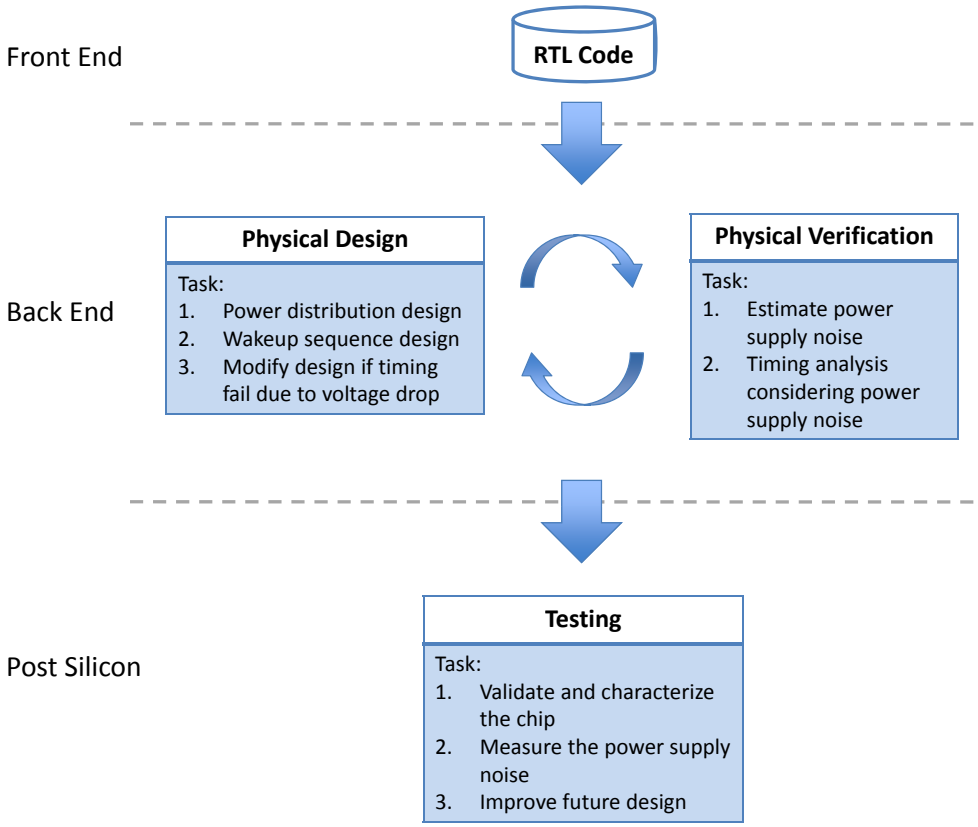


Figure 1.3: Design challenges in different design phases to avoid problem caused by the power supply noise

Table 1.1: Order-of-magnitude variability time scale and estimated delay impact in IBM 65nm technology

Time Domain (secs)	Mechanism	Delay Impact (3 sigma)
1e12	Lithography Node	20%
1e09	Electromigration	5%
1e08	Hot Electron Effect	5%
1e06	Neg Bias Temperature Instability	15%
1e04	Chip Electrical Mean Variation	15%
1e-1	Across Chip L_{poly} Variation	15%
1e-4	Self Heating / Temperature	12%
1e-8	SOI history Effect	10%
1e-10	Supply Voltage	17%
1e-10	Line-to-Line Coupling	10%
1e-11	Residual Source/Drain Charge	5%

1.2.1 Different design techniques to reduce supply noise

Careful physical design is required while implementing the circuit, since it directly determines the quality of power distribution and the timing integrity. There are many approaches to reduce the power supply noise. For example, designers usually widen the power distribution network or insert a huge amount of de-coupling capacitors to provide a robust power network. A better-designed de-coupling capacitor [12][13][14] can also improve the supply quality with less amount of area for capacitors. Supply-noise-aware floorplaning [15][16][17] reduces the voltage drop by reducing current density.

Another major issue designers must take care of is the power gating de-

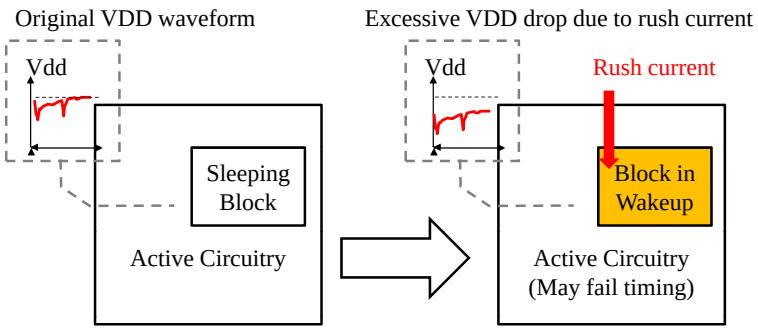


Figure 1.4: Excessive power supply noise due to the rush current

sign. The power gating technique has been widely adopted to reduce leakage current in modern design. However, it also introduces undesirable power supply noise [1][18][19][20]. The *ON* resistances of the sleep transistors cause a higher IR drop in active mode. To avoid an excessive IR drop, the width of the sleep transistor must be sufficient.

Voltage drop during the wakeup phase is another major issue when using power gating techniques. When a sleeping block is activated, it draws a rush current and causes higher IR or Ldi/dt noise than it does during normal operation. This voltage drop may cause the surrounding circuitry in normal operation mode to fail as shown in Figure 6.2. As a result, it is necessary to schedule the wakeup sequence properly to constrain the peak current and to avoid excessive supply noise [20].

1.2.2 Estimate supply noise before tapeout

Power supply noise estimation is crucial to insure the design quality. As mentioned previously, supply noise has a significant impact on timing. An accurate

timing analysis should take power supply noise into consideration. With the power supply noise estimation, the designer is aware of the problem and can go back to modify the physical implementation. Therefore, an under estimation of the power supply noise may cause circuits to fail. On the other hand, an over estimation may cause waste of the design resource, such as routing tracks or area for inserting decoupling capacitor. The importance of considering IR drop and the IR drop model is shown in [21] and in [22].

However, estimating the power supply noise is not trivial, since it is a complex problem of power/current estimation and physical design. Estimating power supply noise involves several issues: (1) how much current is induced, (2) where this current is drawn, (3) when does this current happen, (4) how to model the RLC network, (5) how much RLC is between the switching gates and the power source, and (6) how to simulate the result quickly. There has been extensive research focusing on RLC modeling [23] [24] [25] and the simulation methods [26] [27] [28] to address the issues (4)-(6), but not too many previous works have discussed the issues (1)-(3).

Issues (1)-(3) require finding the circuit activity causing the maximum voltage drop. Random vector simulation may not be the most efficient way to achieve it. For a circuit with N primary input, we need to feed in 4^N input vectors to exhaust all possible combination. Blind search and simulation would be very time consuming and not efficient. There is strong demand to develop systematic and efficient methods to explore the circuit activity causing high supply noise.

A challenging issue is to make a realistic estimation of the supply noise,

which means the circuit activity should be valid through normal function operation. This is because designers care the supply noise under normal operation. An unrealistic estimation, such as the circuit activity during scan mode may be much larger than the normal operation mode. As a result, an over estimation may occur, and design resources may be wasted.

1.2.3 Detect the power supply noise from silicon

After the chip is taped out, designers have to measure the power supply in real silicon to characterize and debug the chip. The measurement results can help designers clarify the reason why the chip does not perform as expected. Moreover, it can also help designers validate the design methodologies to reduce supply noise and improve future projects. The measurement results also can help CAD designers validate and improve the estimation techniques they apply.

Using on-chip detectors is a promising method to measure supply noise. The conventional approach, which measures the power supply noise through the package pins or by capacitive probing, is not effective to capture high frequency noise [8]. An on-chip detector is able to avoid the problem of probing. Different issues occur while designing the on-chip detector. For example, the area consumption of the detectors would be limited. In addition, the calibration of the on-chip detector is another major challenge, since the measured results may vary according to the process, voltage, and temperature variations in the field.

So far, most of the application of the on-chip supply noise detectors are limited to test purpose and are not able to provide immediate alerts for real-time

compensation in normal operation. The major reason of that is the requirement of dynamic calibrations and the off-chip test equipment. As mentioned previously, calibrations are usually required before measurement to obtain an accurate result due to the process and temperature variation. Temperature varies especially, both while the circuit operates and as the ambient condition changes. Manual intrusive operations or other software routines, such as issuing IDLE instructions, combined with the use of off-chip test equipment is usually needed during dynamic calibration. Therefore, dynamic calibration is usually not feasible during normal operation, and this limits the capabilities of detectors providing real-time alerts.

1.3 Contribution

This dissertation focuses on novel techniques to avoid the power supply noise problems. The contributions are summarized as follows.

1.3.1 Develop a method to estimate maximum application-level power supply noise

A methodology is developed, which is able to systematically search for the circuit activity inducing the maximum power supply noise. It first formulates a cost function, considering essential factors, to capture the supply noise caused by specific circuit activities. Powerful search techniques are adopted to explore the circuit activities according to the formulated cost function. Finally, this method uses formal tools to synthesize instruction sequences for those patterns. The power supply noise triggered by this instruction sequence is verified by transient analysis to ob-

tain the voltage drop profile. This method bridges the architecture of the chip with its power distribution network, covering the interactions that span across the entire design. The estimated supply noise is close to the real phenomenon happening in the normal operation mode of a chip.

1.3.2 Design an area efficient on-chip power supply noise detector/evaluator

An area efficient ring oscillator based detector is designed. The purpose of this detector is to facilitate insertion of numerous detectors when there is a need for additional test points, such as a fine-grained power gating design or a circuit with multiple power domains. It focuses on minimizing the area consumption of the detector. This detector can detect and evaluate supply noise on-chip independent of off-chip processing units. The result is evaluated through a dedicated on-chip divider. As a result, the measurement results are available to the power management unit while the circuit is in normal operation.

1.3.3 Design an on-chip self-calibrating power supply noise detector

Another detector equips the capability of self-calibration during normal operation. This detector is robust against process and temperature variations. It requires either no calibration or only a one-time calibration for reducing detection error. Dynamic calibration is not required in any circumstances. This detector is capable of continuously detecting power supply noise and of providing measurement results via a digital output without the need of off-chip test equipment or further processing. With these characteristics, this detector helps not only with val-

idating power supply noise but also provides real-time monitoring during normal functional operation.

1.3.4 Design a dynamic power gating reactivation scheme

A dynamic power gating reactivation scheme is proposed. This wakeup scheme utilizes an on-chip detector which continuously monitors the power supply noise in real time and dynamically controls the wakeup sequence. This technique can protect the active circuitry from the supply noise caused by the rush current during the wakeup phase. If the adjacent active circuit blocks induce an unexpectedly high voltage drop, the wakeup sequence is held and the overall power supply noise is constrained beneath an established threshold even when the adjacent active circuit blocks induce an unexpectedly high voltage drop. Moreover, this scheme also speeds up the wakeup sequence while the ambient voltage drop is low. As a result, this wakeup scheme utilizes the voltage margin more efficiently during the power gating reactivation.

1.4 Outline of this dissertation

The dissertation is organized as follows. It starts with a literature review of existing work on power supply noise in Chapter 2. The method estimating the application-level power supply noise is explained in Chapter 3. The two on-chip power supply noise detectors are described in Chapter 4 and Chapter 5 respectively. The dynamic power gating reactivation scheme is introduced in Chapter 6. In Chapter 7, a summary of the contribution is presented and the future directions

are discussed.

Chapter 2

Survey of existing techniques preventing power supply noise problems

This chapter presents several existing techniques to avoid the problems caused by power supply noise in estimation, on-chip detector design, and power gating reactivation three categories.

2.1 Estimation methodologies

Several methodologies have been proposed for finding the circuit event triggering peak power [29][30][31][32][33][34]. However, these techniques do not focus on estimating the voltage drop, but rather stop with estimating the peak power. The power distribution network is not taken into account and the circuit activity event may not generate the maximum power supply noise.

The method proposed in [35] uses the strategy in [36] to compose the current waveform. Based on the composed waveform, a quick supply noise simulation is performed to examine the quality of the generated activity. This method takes several iterations to refine the searched circuit activity. Another work presented in [37] proposes a method to estimate a lower bound of power supply noise by considering only the Ldi/dt noise. This method first generates a pattern through ATPG

to identify the transient current characteristics. The maximum transient current is found by a greedy heuristic. Both of these approaches do not validate the circuit activity with the functionality in normal operation. Thus, the generated sequence will result in an unrealistic estimation [38].

Another type of strategy maximizes the mid-frequency supply noise. The method in [39] synthesizes the global current waveform inducing the min-to-max current. The method presented within [40] adopts the Wavelet-based analysis to characterize the current profile in both the time and frequency domains. Both of these approaches do not consider the validation of the current profile through instruction execution. An unrealistic estimation may occur. The method in [2] considers the validation of circuit activity through instruction streams. It first characterizes the current for each atomic operation. The connectivity between these atomic operations is analyzed and the instruction stream is synthesized to maximize the RLC resonant noise. These three strategies consider only mid-frequency noise. On-chip IR effect and the high frequency noise are not taken into account.

Another type of strategy [41][42] does not generate any specific activity event but performs static (vectorless) analysis. This type of strategy takes the probabilistic approach to construct the current waveform. This approach is now widely adopted in commercial tools, since it avoids the problem searching the circuit activity. Nevertheless, this type of analysis may not be able to capture the worst case supply noise.

Reviewing these existing methods, some of them perform blind search. Some of them do not consider all of the essential factors while formulating the

cost function. A more comprehensive cost function is needed in order to perform a more efficient search. Moreover, most of them do not consider the validation of generated circuit activity in normal function mode. For a processor level design, a valid circuit activity in normal function mode means this event can be triggered by instruction execution. It is important to note here that *not* all localized patterns are achievable or reachable through instructions. In fact, only a few of the localized patterns can be reached through instruction execution and it depends on how deep our signals of interest reside in the pipeline of the processor.

The method presented in Chapter 3 develops a comprehensive cost function capturing the voltage drop induced by specific circuit activities. It utilizes a systematic approach to explore the circuit activity maximizing power supply noise while the activity satisfies both physical and functional constraints. As a result, the voltage drop induced by the found activity is a realistic estimation.

2.2 On-chip detectors

There has been extensive research in designing on-chip power supply noise detectors. Ring oscillator based supply noise detectors were proposed in [43] and [44]. The ring oscillator frequency varies according to the local supply voltage. Hence, supply noise can be detected by counting the number of cycles within a certain amount of time. This type of detector has the benefit of low design cost. However, the area cost is still considerable while numerous detectors are required. Moreover, these detectors usually are not feasible to detect a high-frequency noise.

Another ring oscillator based detector is proposed in [11]. This detector in-

tends to improve the time resolution by using a sample-and-hold circuit to capture instantaneous supply noise. This captured voltage value is used to drive an analog buffer and provide the power source to a ring oscillator. This detector significantly improves the time resolution for a ring oscillator based detector. Nevertheless, this detector can perform only single-shot detection within a very long time. A huge amount of duplicated measurements and off-chip processing are required to construct the voltage waveform. In addition, the area consumption is significant for this detector.

Two different types of detectors are proposed in [45]. One uses a source follower to sense the local VDD and uses a latch comparator to compare the sensed VDD to an ideal voltage source. This detector is able to detect high resolution supply noise but requires considerable area. The other detector also uses a source follower to sense the local VDD but uses a transistor as transconductance to convert the voltage to current. A current mirror delivers the current to an off-chip current meter, and the local VDD can be detected by measuring the current. This detector is very small and high resolution can be achieved. However, the result is measured as current through off-chip equipment. Hence, it can not provide any information to the power management unit while the circuit is in normal operation.

Another detector in [3] detects supply noise by observing differential current variation. First, a reference current generator generates a pair of reference currents. Two digital-to-analog convertors (DACs) are used in the current generator unit to calibrate process, voltage, and temperature variations and to tune the threshold voltage. The resolution in voltage and time domains of this design is good. However,

the area penalty of this design is high, and careful calibration is required. Another similar approach [8] use a smaller DAC to reduce the area overhead. A bandgap reference is used to generate the clean VDD. This design sacrifices the noise bandwidth to reduce area consumption, but careful calibration is still required.

A process and temperature insensitive detector is proposed in [46]. This detector use two identical process and temperature insensitive delay lines to detect supply noise. A RC low pass filter is required to stabilize the clean VDD. However, this detector compares local VDD to the clean VDD. Therefore, only overshoot or undershoot information can be obtained.

Existing on-chip detector designs can be roughly classified into two categories, ring oscillator based detector and comparator based detector. Ring oscillator based detectors, illustrated in Figure 2.1 usually can detect supply noise as an absolute value output but can detect only low-frequency noise. The area consumption is considerable if multiple detectors are placed within a chip. Comparator based detectors, illustrated in Figure 2.2 and Figure2.3, compare the local supply voltage value to a pre-determined reference voltage or reference current. Therefore, most of the comparator based detectors can detect only overshoot/undershoot with respect to a reference voltage level within a single measurement. On the other hand, most of the detectors of both types mentioned above require dynamic calibration before measurement to obtain accurate results.

The detector presented in Chapter 4 of this dissertation reduces the area consumption of the ring oscillator based detector. The area cost is minimized when there is a need for numerous detectors within a chip. The detector presented in

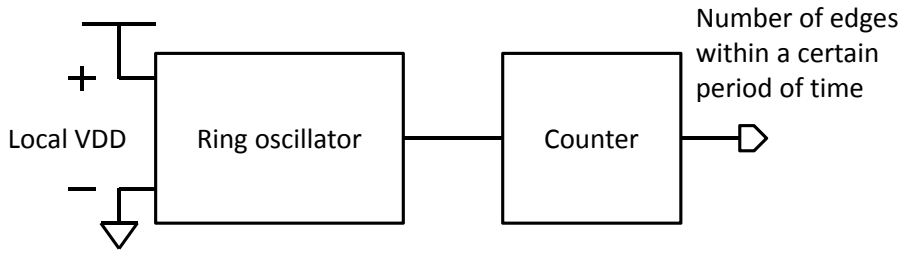


Figure 2.1: Typical ring oscillator based detector

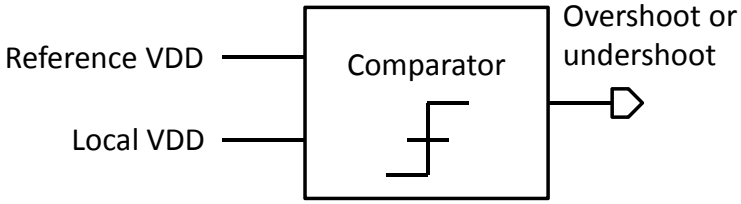


Figure 2.2: Detect supply noise by comparing the local VDD to a reference voltage source

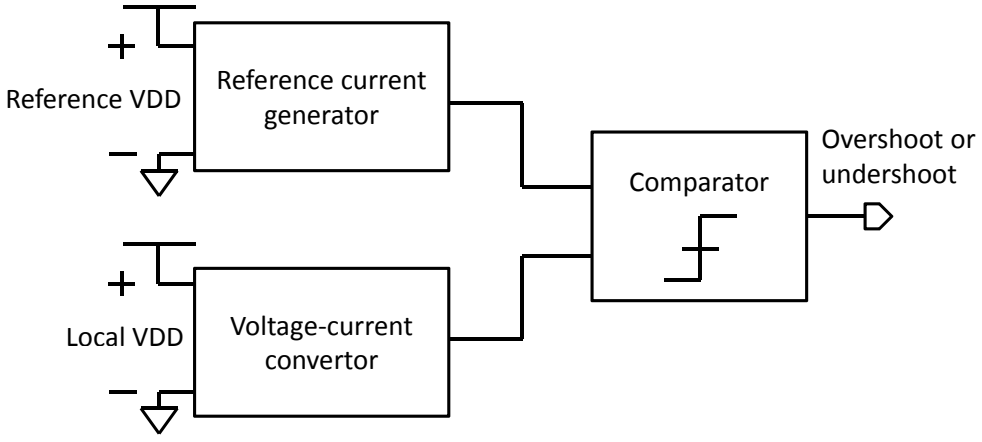


Figure 2.3: Convert voltage to current to detect supply noise

Chapter 5 performs self-calibrations, and no calibration is required before measurement. Moreover, this detector is capable of continuously detecting power supply noise in real time. The measurement results are generated as a digital output, which carries more information than simple overshoot/undershoot. Consequently, only one-time measurement is sufficient to construct the real supply noise waveform.

2.3 Reactivation methodologies of power gating technique

Previous research has been proposed to reduce power supply noise during the wakeup phase. The basic principle behind all of these methods is to turn on the sleep transistors gradually to constrain the rush current. Two different reactivation schemes are proposed in in [47]. The first scheme connects all of the sleep transistors as a single transistor, but the TURN_ON signal is raised gradually as shown in Figure 2.4. The rush current is constrained by the Vgs ramp of the sleep transistor. The second scheme uses parallel sleep transistors and inserts delay elements within the propagating path of the TURN_ON signal as illustrated in Figure 2.5. The delay of each delay element and the size of each sleep transistor can be varied to arrange the best wakeup sequence. In this type of scheme, the current is constrained by the total sizing of the ON sleep transistors.

A similar approach is presented in [48], which uses a two-level approach. The sleep transistor is first driven by a very weak gate. In this approach, the rush current is limited by raising the Vgs slowly. After the virtual VDD almost reaches the full VDD level, the strong driver is turned on and raises the virtual VDD quickly without drawing excessive rush current.

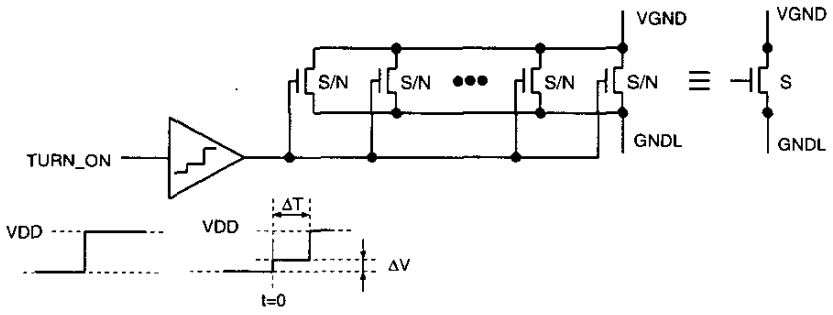


Figure 2.4: A sleep transistor or a set of sleep transistors whose VGS increases in a non-uniform stepwise manner

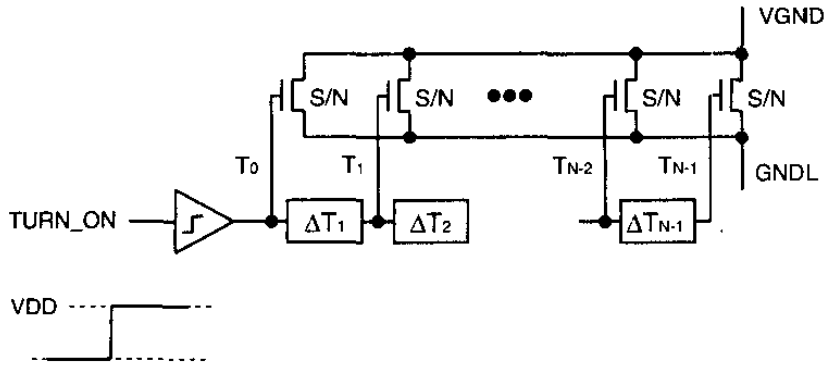


Figure 2.5: A portion of sleep transistor that is switched on increases in non-uniform stepwise manner

The work in [49] uses an algorithm approach to systematically determine the step of wakeup sequence. This approach ensures that the sleep transistor delivers a desired current and follows the current constraint (power supply noise constraint). The current constraint is predetermined and ensures the maximum possible power supply caused by the rush current. The size of each step is optimized through the proposed algorithm. Another algorithm approach is presented in [50]. This approach develops an algorithm for a multi-power-domain design. The power up sequence is arranged to reduce the overall power supply noise.

These aforementioned methods are able to effectively reduce power supply noise caused by the rush current. However, these methods are all designed as a predetermined wakeup sequence according to the worst case situation. Those methods are not able to adjust the wakeup sequence according to the ambient condition in real time. Inevitably, these methods need to leave considerable margin and do not achieve optimal solutions.

This approach utilizes an on-chip voltage monitor to detect the local voltage level. The Vgs of the sleep transistor is dynamically controlled according to the local voltage. However, this method also can not avoid the excessive voltage drop when an un-predicted high supply noise is induced by the active circuitry. For all of these aforementioned techniques, a larger design margin must be added, to account for an unpredicted high voltage drop caused by burst circuit block operations.

A previous work in[51] proposes a dynamic power-up scheme. This approach utilizes an on-chip voltage monitor to detect the local voltage level. The Vgs of the sleep transistor is dynamically controlled according to the local voltage.

This method is able to reduce the wakeup time and the voltage resonant time during the wakeup phase. However, it can not avoid the excessive voltage drop, when the active circuitry induces an un-predicted high supply noise during the wakeup sequence.

The presented dynamic power gating reactivation scheme in Chapter 6 monitors power supply noise in real time. It is able to dynamically adjust the wakeup sequence according to the ambient voltage. This wakeup scheme suppresses the supply noise caused by the rush current while an unpredicted high voltage drop is induced by other active circuitry.

Chapter 3

Estimation of maximum application-level power supply noise

As mentioned previously, an accurate estimation of power supply noise has a crucial impact on design quality. To predict and avoid excessive voltage drop, this chapter presents a new methodology that systematically searches and generates the activity inducing the maximum power supply noise. The strategies behind the cost function formulation and how to search an instruction-valid vector to trigger maximum power supply noise will be described.

3.1 Background

Several metrics are used to analyze the effects of power supply noise [52]. Static voltage drop indicates the average supply noise within a circuit and can provide quick and rough information on the power distribution quality. However, it does not contain high frequency supply noise information, since it does not capture the real voltage waveform of a circuit. Dynamic voltage drop indicates the voltage waveform including the peak instantaneous drop at any point of time within a clock period for the circuit under study. Transient analysis is required to obtain the dynamic voltage drop, and annotating it into timing analysis is difficult. Cycle-

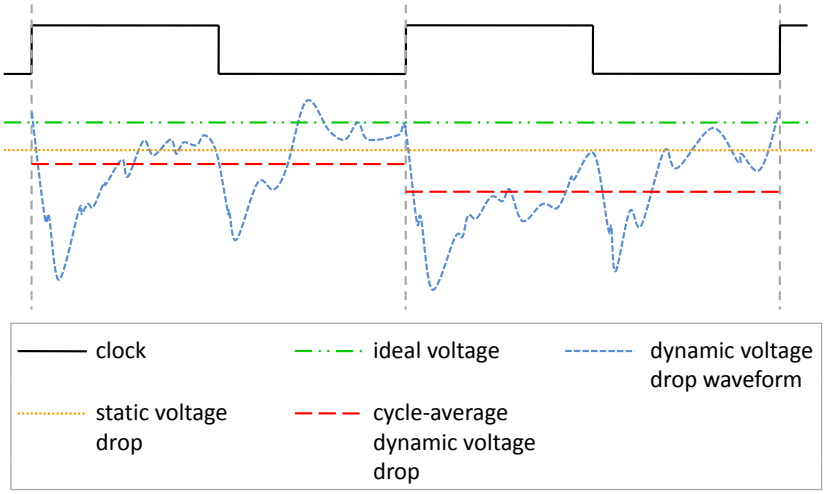


Figure 3.1: Several metrics while evaluating the power supply noise

average dynamic voltage drop indicates the average dynamic voltage drop for a clock period. It is also easier to be annotated into timing analysis and is sufficiently accurate. These metrics are illustrated in Figure 3.1. In this chapter, this approach estimates the cycle-average voltage.

3.2 Methodology

The goal of this work is to find the event that causes the maximum cycle-average dynamic voltage drop while the processor is executing instructions. The approach taken to solve this problem consists of the steps shown in Figure 3.2. The input to our methodology is the placed and routed design of the chip, together with its power distribution network. Based on the power report of the cells and the power distribution report, the cost function is formulated. This cost function is maximized

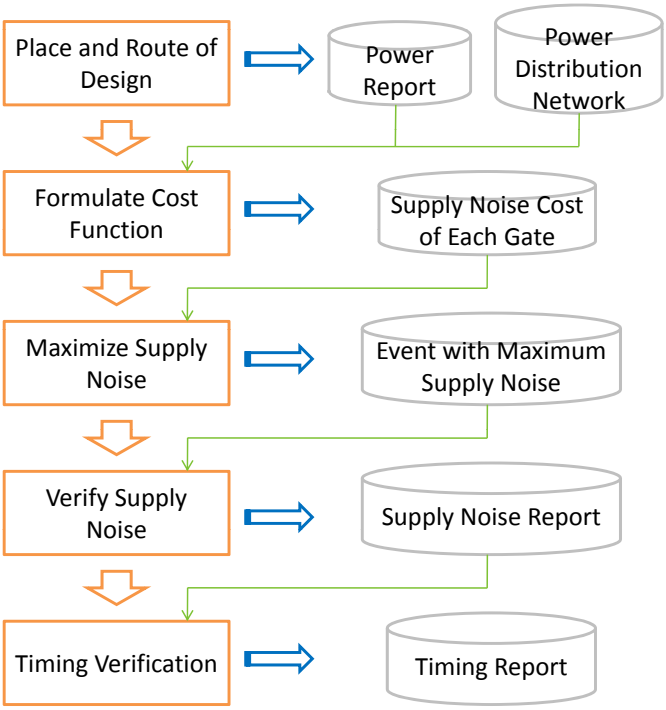


Figure 3.2: Estimation of maximum supply noise

through efficient search techniques. The output of the search technique is simultaneously verified for functionality, by using formal techniques. The instruction sequence obtained from the formal technique is simulated with the power distribution network for estimating the voltage drop. The methodology is discussed in tatil in the next section.

3.2.1 Cost function formulation

To identify the priority of the cells to be toggled, a cost must be associated with each cell's instance. The higher the formulated cost, the greater is the contribution of the cell towards voltage drop. This proposed cost function considers the IR effect, the inductance effect and the region selection in formulating the cost function for each cell, as follows.

3.2.1.1 IR effect

The factors contributing to the IR effect are the switching current of the cell and the effective resistance of the power grid connecting the power source to the cell. The switching current of each cell is determined by using the power analysis tools on the placed and routed netlist. The effective resistance for each cell is modeled according to its physical location and power distribution.

The purpose of this model is to maximize the overall voltage drop in a larger area of the chip, and not to maximize the voltage drop in a few cell rows. This is because the maximum voltage drop in a few cell rows does not equate to the maximum delay increase of the associated paths, as the gates and nets involved in

that path are usually spread across numerous cell rows. Therefore, the effective resistance of each cell instance considers only the power ring and the power mesh. The resistance of the power rail is not taken into our consideration, as it is a local effect.

The effective resistance model is illustrated in Figure 3.3 and it can be observed that the cells sharing the same power mesh have the same effective resistance. For example, the cell A and cell B has the same effective resistance ($R_{effective}$), since they share the same power mesh. The $R_{effective}$ of cell C is different from the $R_{effective}$ of cell A and cell B, though the cell C is also sitting on the same row with cell A and cell B. This is because the cell C does not share the same power mesh with cell A and cell B. The cost metric for each individual cell instance due to the IR effect is formulated in Equation 3.1.

$$IR_{cell}(i) = I_{cell}(i) \times R_{cell}(i), \tag{3.1}$$

where $IR_{cell}(i)$ is the cost metric of a cell i due to its IR drop, $I_{cell}(i)$ is the component due to switching current and $R_{cell}(i)$ is the effective resistance of the cell.

3.2.1.2 Inductance effect

The inductance of the power distribution network is mainly contributed by the package. The voltage drop caused by an inductor depends on the rate of change of current on it. When there is a sudden and huge difference in the amount of capacitance being switched, as in mode changes (e.g., idle $\rightarrow$ normal), the inductive noise

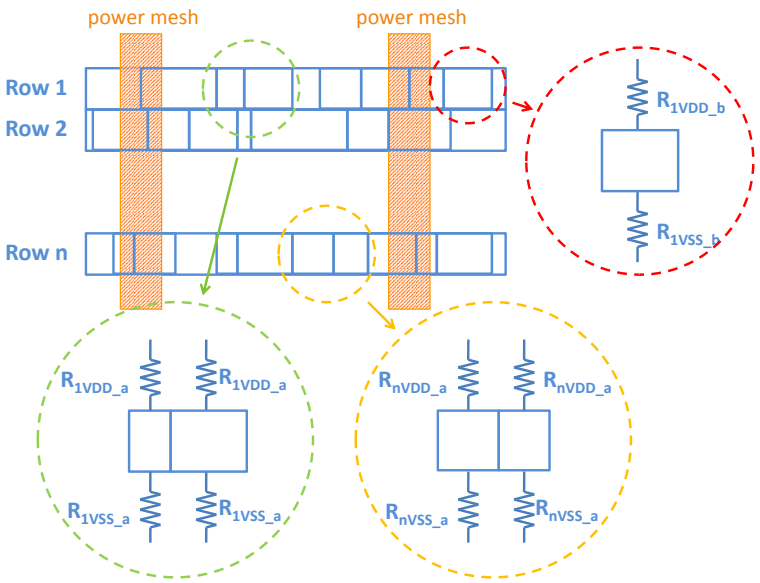


Figure 3.3: Effective resistance model for IR effect

is high. However, this effect can be easily simulated, as the instruction sequence causing the mode changes of the processor is usually known. Since the purpose of the proposed method is to find the unknown circuit activity event triggering the maximum supply noise during normal operation, the power mode change is not formulated in the cost metric.

For the test circuit design in the experiment, the current boost on the package happens after the clock edge during normal operation and causes the $L * \frac{di}{dt}$ drop. To maximize the simultaneous peak current around the desired time period, the $L * \frac{di}{dt}$ cost of each cell instance is evaluated by the magnitude of the switching current and the corresponding switching window. More specifically, cells with higher current usage and those that switch around the clock edge are given higher weight. For

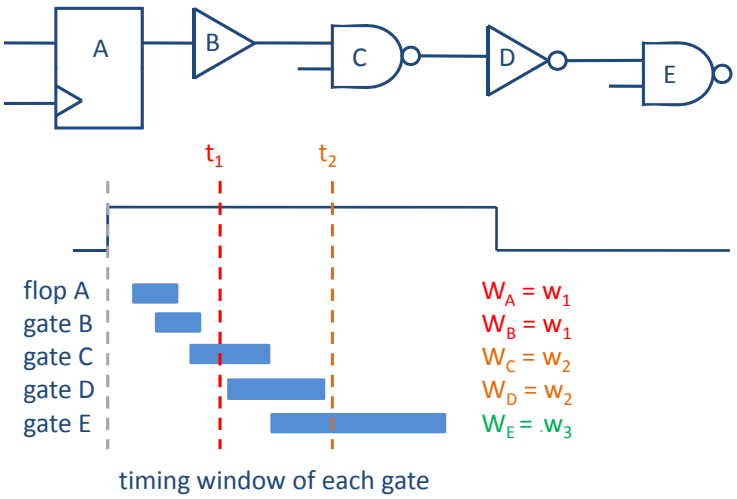


Figure 3.4: Weighting for cells switching at different times

example, assume that the timing window of interest is between the clock edge and the time t_1 to maximize the $L * \frac{di}{dt}$ as shown in Figure 3.4. The cells switching within this window (flop A and gate B) are given higher weight w_{t1}, and cells out of this window will be given comparatively lower weights w_{t2}, ..., w_{tk}. This method enables us to allow multiple weightings on multiple timing windows. The weighting can be adjusted according to the characteristic of a design. The cost metric for this component of inductance effect $L_{cell}(i)$ is formulated in Equation 3.2.

$$L_{cell}(i) = I_{cell}(i) \times W_{cell}(i), \begin{cases} W_{cell}(i) = w_{t1}, & \text{for} \quad t_{switch} < t_1 \\ W_{cell}(i) = w_{t2}, & \text{for} \quad t_{switch} < t_2 \\ \qquad\qquad ... & \\ W_{cell}(i) = w_{tk}, & \text{for} \quad t_{switch} < t_k \end{cases} \tag{3.2}$$

3.2.1.3 Region selection

The region selection metric is based on the implementation of the design, specifically on the location of the cells. This cost metric provides a method to trigger more activity in our region of interest, e.g., the region potentially with higher voltage drop or which is timing critical. The strategy involved in selecting this region is highly dependent on the floorplan and on the power plan. It also depends on whether the chip uses the wire-bond or the flip-chip package style. Knowledge about these details of the design is crucial in making a good decision on region selection.

For a design with a wire-bond package, the power and signal pads are located at the four sides of the chip along its periphery. Assuming that the power distribution network is evenly spread across the chip, the maximum cycle-average voltage drop usually occurs in the middle. Therefore, the cells which are located closer to the center should have a higher priority to be toggled to maximize the voltage drop.

For a design with a flip-chip package, the power pads are spread evenly across the whole chip. It is not obvious to locate the region with the maximum drop intuitively. More knowledge about the design and its floorplan can help to make the decision. Designers typically need to know where the power-hungry parts of the chip are tiled out, to select the region of preference.

When a region is given more preference, the surrounding region should also be given a higher weight. There are two reasons supporting this approach. First,

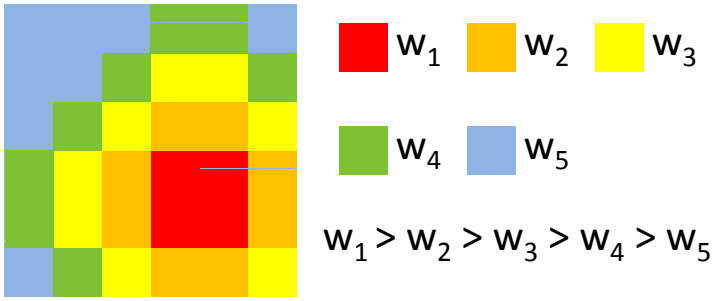


Figure 3.5: If R1 is the region of interest, cells in selected and surrounding regions are weighted as: $s_1 > s_2 > s_3 > s_4 > s_5$

circuit activity in the nearby region will contribute more voltage drop compared to the activity in the far off regions. Second, the cells within the surrounding area are usually more functionally related. Favoring to trigger the cells within the surrounding area helps to trigger the cells in the targeted area. This approach is illustrated in Figure 3.5. In the figure, region R_1 is our region of interest. Therefore, cells within this region are given a higher weight (s_1), and cells within the surrounding region R_2, R_3, R_4, and R_5 are given descending weights s_2, s_3, s_4, s_5. The cost metric of each cell $S_{cell}(i)$ is formulated in Equation 3.3.

$$S_{cell}(i) = \begin{cases} s_1, & \text{for} \quad cell(i) \in R_1 \\ s_2, & \text{for} \quad cell(i) \in R_2 \\ \ldots & \\ s_k, & \text{for} \quad cell(i) \in R_k \end{cases} \tag{3.3}$$

3.2.1.4 Overall effect

Combining the three cost metrics previously described, the overall power supply cost for each cell instance is formulated in Equation 3.4.

$$\begin{aligned} C_{cell}(i) &= region\_selection\_cost \times [k \times IR\_cost \\ &\quad + (1-k) \times inductance\_cost] \\ &= S_{cell}(i) \times [k \times (I_{cell}(i) \times R_{cell}(i)) \\ &\quad + (1-k) \times (I_{cell}(i) \times W_{cell}(i))] \end{aligned} \tag{3.4}$$

Here, each cell instance has its own $S_{cell}(i)$, $I_{cell}(i)$, $R_{cell}(i)$, and $W_{cell}(i)$ weights corresponding to its region, current, physical location, and switching time respectively. The k factor is a global parameter to evaluate the weighting ratio between the IR effect and the $L * \frac{di}{dt}$. The necessity of the k factor is because of the difficulty in quantifying the impact of each individual cell transition on voltage drop while considering the inductance effect. In order to fairly consider the IR effect and the inductance effect, this k factor is added into the cost function formulation. The value of the k factor is determined through the characterization process described in Section 3.2.1.5.

The overall voltage drop cost for the entire chip corresponding to the transition of each instance is formulated in Equation 3.5, which is also the objective function. In Equation 3.5, $T_{cell}(i) = 1$ if the cell i is switching, and $T_{cell}(i) = 0$ if the cell i is not switching. The goal is to find the circuit activity event ($T_{cell}(i)$ vector) maximizing the overall cost (described in Section 3.2.2).

$$Overall\ cost = \sum_{i=0}^{gate\ count} C_{cell}(i) \cdot T_{cell}(i) \tag{3.5}$$

3.2.1.5 Characterization of parameters

Revisiting the cost function in Equation 3.4 and 3.5, the current component $I_{cell}(i)$ and the resistance component $R_{cell}(i)$ are deterministic. Only $S_{cell}(i)$, k, and the $W_{cell}(i)$ factors need to be characterized (one time). This is similar to an unconstrained optimization problem. To characterize and obtain a satisfactory set of weights for the cost function, an optimization technique in [53] is adopted to perform the characterization. This strategy starts the search from a best known approximating point and takes an iterative approach searching for the optimal solution along the conjugate directions. This method ensures that the convergence rate is always efficient even if we start from a bad initial point [53]. The required search for each iteration is linear to the number of variables within the function. In this work, the parameters were characterized within two iterations. More details are discussed how the cost function is maximized and how the instruction sequence drawing the maximum voltage drop is obtained in the next section.

3.2.2 Maximization of cost function and validation with instructions

To maximize voltage drop, the cost function (Equation 3.5) should be maximized. To maintain the validity of the vector sequence maximizing the cost function, it should be periodically verified for functionality. An efficient search technique and a hierarchical verification approach in checking the validity of the vector

sequence is described in [34] and [54].

Reactive tabu search is used for maximizing the cost function [55]. Reactive tabu search consists of two search techniques meshed together. The first search (local search) searches locally from the starting configuration, and identifies the maximum in the neighboring search space. The second search (tabu search) has a prohibition list and it uses this list to make sure that it does not visit previously visited configurations [56]. Reactive tabu search has been compared for its effectiveness with best known search techniques and is formally sound [57].

As discussed before, the configurations must pertain to circuit functionality. A hierarchical verification approach is used to check the validity of the vector sequence. The instruction constraint is formulated and is used to verify the validity of the circuit activity at the highest level. The combined constraint is then negated, coded into an assertion and is fed to a formal verification tool (Cadence SMV [58], Synopsys Magellan [59]) to check if this assertion has a counterexample. If a counterexample exists that falsifies the assertion, then it is formally proved that there exists a valid instruction sequence that sets and excites all the nodes in that configuration. Next, we detail the steps to obtain the voltage drop from this instruction sequence.

3.2.3 Power grid analysis

Transient analysis needs to be performed for the activity event generated by our search and instruction synthesis technique to capture the dynamic voltage drop information. However, transistor-level simulation usually takes an extremely

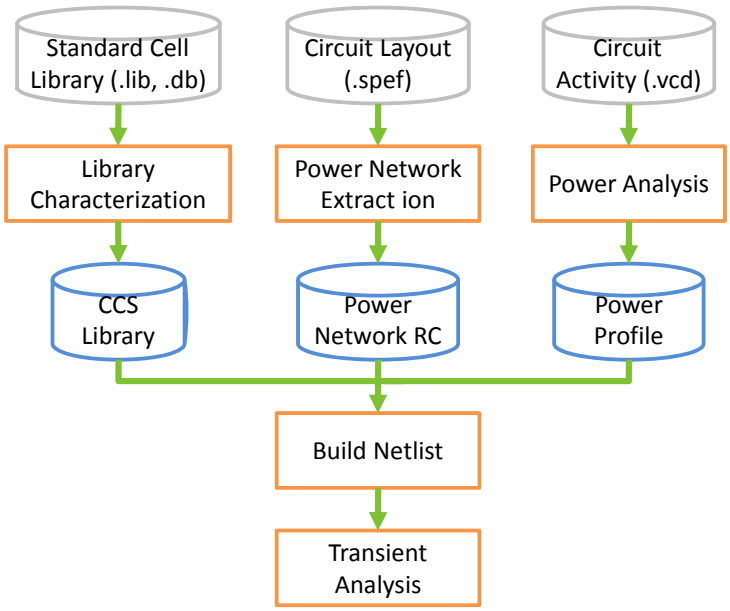


Figure 3.6: Power grid analysis procedure

long time. To reduce the simulation time, the transistor level gates are replaced by the Composite Current Source (CCS) model. After an instruction-valid circuit activity is obtained by using the method described previously, the power and current profile of the activity event is analyzed. The CCS netlist is generated according to the power profile and the extracted power distribution network. As a result, the simulation time can be reduced without sacrificing the accuracy, since the detailed power distribution network information is kept within the CCS netlist. The analysis procedure is shown in Figure 3.2.3.

3.3 Results and discussion

3.3.1 Experiment setup

The test circuit in the experiments is the Open-RISC processor (OR1200) implemented in the TSMC 0.18*um* technology. Synopsys ICCompiler was used to perform the place and route, and to extract the RC values in the power distribution network and standard cells. Synopsys PrimeTime PX was used to characterize the event-based current profile from the instruction sequence, and Synopsys Primerail environment was used to analyze the power distribution network and to build the CCS netlist. We used Synopsys Nanosim for the transient analysis of the test circuit for the instruction sequence.

The test circuit is implemented with both wire-bond and flip-chip package styles. In the experiment, it is assumed that the voltage regulator is an ideal voltage source and the power distribution on the motherboard is ideal as well. Hence, the simulated supply noise is caused by only package and the within-die power distribution.

Synopsys Primerail is used to perform the static analysis (vectorless simulation) on power supply noise as our reference. Also, random simulation executing the add instruction is also performed to be another reference. This is because the add instruction generally induces higher supply noise in the test circuit than all other instructions do, to the best of our knowledge. Therefore, those random vectors have a better chance to induce the maximum power supply noise.

3.3.2 Wire-bond design

In the wire-bond design, the VDD and VSS pins are located at the four corners of the chip. The cycle-average dynamic voltage drop profiles obtained for different combinations of cost metrics used in formulating the cost function are shown in Figure 3.7. Figure 3.7(a) shows the voltage drop obtained from a vectorless simulation in PrimeRail. Figure 3.7(b) shows the worst case voltage drop from executing 2000 random vectors while executing the add instruction. Figure 3.7(c) shows the voltage drop profile of the instruction sequence obtained when maximizing power by using our method. Figure 3.7(d) shows the voltage drop profile of the instruction sequence considering the IR, the inductance, and the region selection effects which also generates the maximum voltage drop.

More detailed cycle-average voltage drop results for the instruction sequences obtained by considering different cost functions are shown in Table 3.1. Column one and two list different methods of simulation. Column three lists the values of the cycle-average voltage drop averaged across the chip, and column five lists the peak cycle-average voltage drop of the chip. Columns four and six are the normalized values with respect to that of the static case. The following observations can be made from these results.

1. The voltage droop estimated through vectorless static analysis is relatively low compared to other approaches. This is because the static simulation is a probabilistic approach and reflects only an average voltage drop. Therefore, the vectorless static simulation is not sufficient for power supply noise

estimation

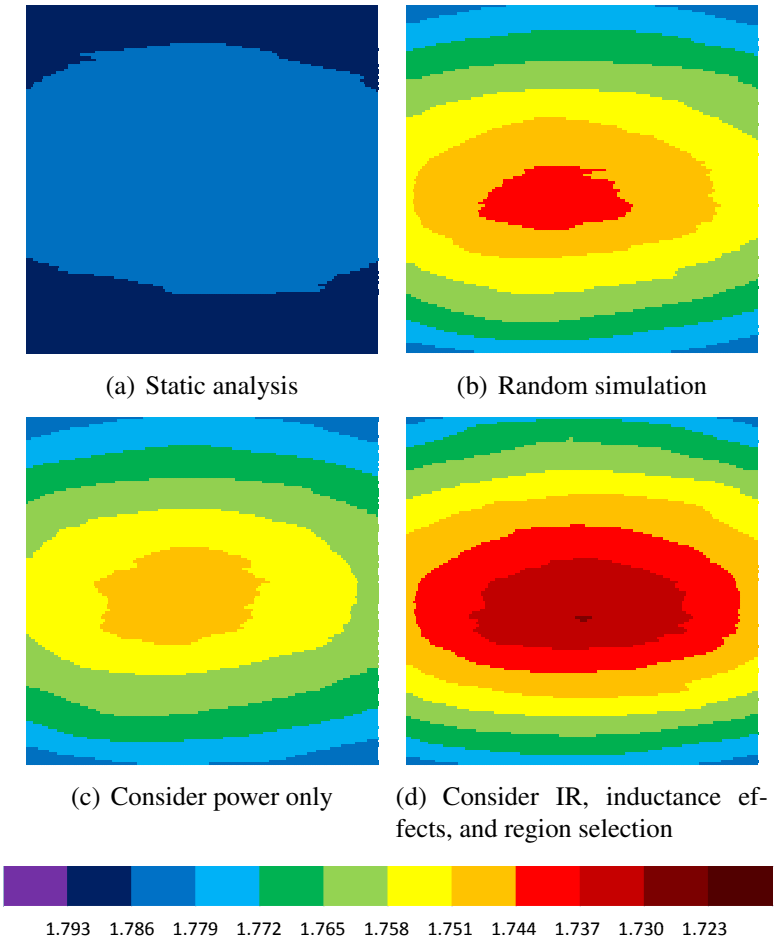
2. Our method can generate the maximum supply drop (91mV) when we consider all the cost metrics discussed in Section 3.2. Maximizing for peak power is not enough while predicting the maximum power supply noise, since it does not consider the physical and the timing factors of the circuit activity. The circuit activity maximizing the peak power generates only a 64mV drop, which is even lower than the random vectors simulation in our experiment. This proves the effectiveness of our cost function formulation.

3. Though random simulation generates a larger voltage drop (74mV) compared to static analysis in our experiment, there is a chance that the random vectors may or may not achieve a high voltage drop within a limited number of trials. In addition, the long run time of the simulation (Section 3.3) makes the random simulation unattractive.

3.3.3 Flip-chip design

For the flip-chip package style, similar experiments are also performed to validate the effect of the cost metrics. The results are shown in Figure 3.8. The voltage profiles of the static analysis and the worst voltage drop from random simulation are in Figures 3.8(a) and 3.8(b).

In order to determine the region of interest for the region selection cost in the cost function, the proposed method is first performed with only the power cost within the cost function. According to the result, the region with the worst supply



(a) Static analysis

(b) Random simulation

(c) Consider power only

(d) Consider IR, inductance effects, and region selection

Figure 3.7: Voltage drop maps with different cost function formulation

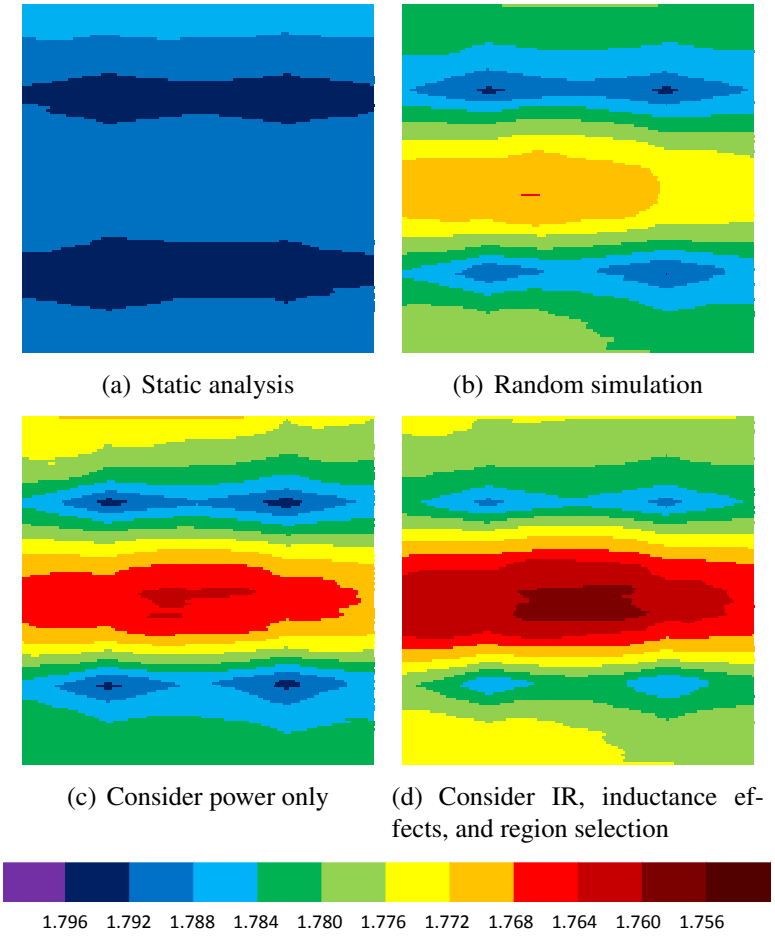
Table 3.1: Average and maximum cycle-average voltage drop for different cost function formulation in wire-bond style design

Different simulation methods		Avg Drop		Max Drop	
		mV	Normalized	mV	Normalized
Static analysis		10.9	100%	16.1	100%
Random simulation		48	440%	74	459%
Our method	Maximizing power only	44	404%	64	398%
	IR, inductance, and region selection	59	541%	91	565%

noise can be predicted as in Figure 3.8(c). From Figure 3.8(c), it can be clearly seen that the center and the left center regions are potentially the regions with high voltage drop. Therefore, this region is given a higher weight while the complete cost function is formulated. The result of the complete cost function is shown in Figure 3.8(d). From Table 3.2, it can be concluded that the cost function formulation method is also effective for the flip-chip package style design in maximizing the supply drop, as it gives a higher drop (58mV drop) when compared with that of random simulation (42mV drop).

3.3.4 Run time

The run times for static analysis, random simulation, and the proposed method are listed in Table 3.3. The first and second columns show the simulation method, and the third column shows the required time to finish the simulation. The simulation time for a single clock cycle on the CCS netlist takes seven minutes



(a) Static analysis

(b) Random simulation

(c) Consider power only

(d) Consider IR, inductance effects, and region selection

Figure 3.8: Voltage drop maps with different cost function formulation

Table 3.2: Average and maximum cycle-average voltage drop for different cost function formulation in flip-chip style design

Different simulation methods		Avg Drop		Max Drop	
		mV	Normalized	mV	Normalized
Static analysis		8	100%	17	100%
Random simulation		24	300%	42	247%
Our method	Maximizing power only	27	338%	50	294%
	IR, inductance, and region selection	33	413%	58	341%

(executing one instruction per cycle). Therefore, the run time for the random simulation is extremely long. From the Tables 3.1, 3.2, and 3.3, the proposed method can reach a higher supply drop ($> 20\%$) when compared to that of random simulation in approximately 4% of the run time.

3.4 Summary

This chapter has presented a methodology to estimate the maximum supply drop and its effects at the application-level using a sequence of instructions. This is achieved by formulating the cost function considering different cost metrics and using efficient search techniques to maximize the cost function. From the results, it is necessary to consider the resistance of power supply network, region selection and inductance effect within the cost function. The vector sequence that maximizes the cost function is verified for functionality and associated with instructions using formal tools. This way, the estimate is realistic and the sequence of instructions can

Table 3.3: Run time comparison between static analysis, random vector simulation, and our method

Simulation Method		Run Time (min)
Static analysis		2
Random simulation on CCS netlist (2000 instructions)		14000 (7/per vector)
Our method	Search and generate activity	420
	Simulation on CCS netlist	56 (7/per vector)

be included as part of a system-level verification set for supply drop.

To verify the quality of this estimation methodology, on-chip detectors are required to monitor the voltage drop in the fabricated chip. In the next two chapters, two on-chip power supply noise detectors are introduced, which are able to validate the power supply estimated by this approach.

Chapter 4

An area efficient on-chip power supply noise detector/evaluator

In the last chapter, a methodology was introduced to estimate the maximum power supply noise. This chapter and the next chapter will introduce two different on-chip detector schemes which are able to verify power supply noise after the chip is fabricated. This chapter will present an area efficient power supply noise detector/evaluator based on a ring oscillator approach. The idea of area minimization and the on-chip evaluation will also be explained. Post layout simulation results will be demonstrated as well.

4.1 Ring oscillator based detector scheme

A ring oscillator has been commonly used as the process monitor. Its supply voltage controlled frequency serves as a simple way to detect supply noise. A ring oscillator based detector proposed in [43] consists of a m-bit wide chip clock counter (CCC), n-stage ring oscillator, and a p-bit wide ring oscillator counter (ROC), as shown in Figure 4.1. The CCC determines the timing window when the detector circuit operates. The window is set by an m-bit wide setup signal. Once the CCC receives the enable signal, it will start counting the number of cycles of

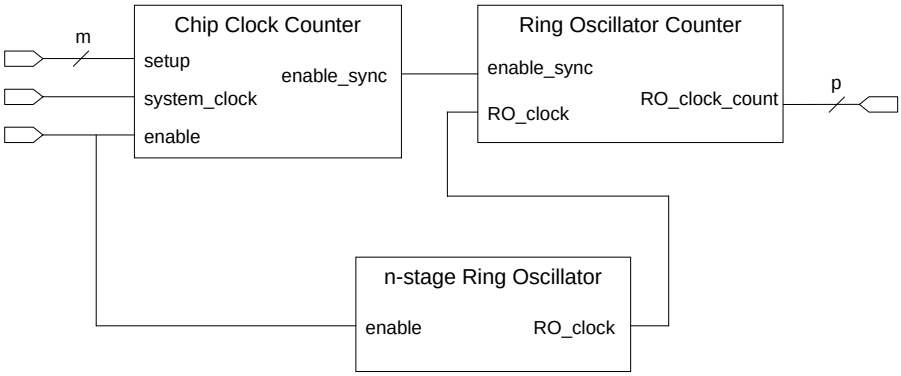


Figure 4.1: Ring oscillator based power supply noise detector

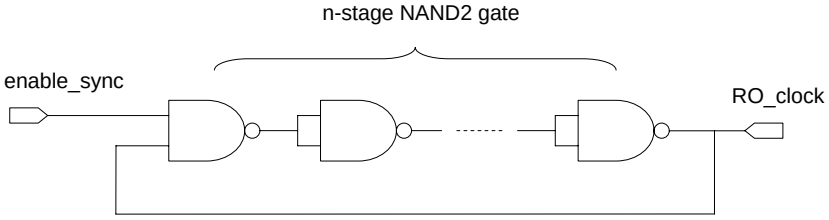


Figure 4.2: N-stage of NAND2 gate ring oscillator with enable signal

the chip clock, while enabling the ring oscillator. The ring oscillator consists of n-stage of NAND2 gates, as shown in Figure 4.2. Once enabled, the ring oscillator will generate a clock signal with a certain frequency according to the local supply voltage. The clock signal will trigger the ROC to start counting rising edges generated by the ring oscillator. A synchronized enable signal generated by the CCC enables the ROC, in order to count the clock edge in a window specified by setup. The control unit stops the ring oscillator when the CCC's count reaches the end of the window. The ROC's value reflects how many clock edges are generated.

The ring Oscillator's frequency will vary due to process variations, as well as local voltage level, causing the final value of the ROC to differ from detector to detector under the same operating conditions. To account for the process variation affecting the frequency of the RO, every detector is first operated while suppressing all other activity on the chip. The voltage drop ratio can be calculated from the ratio of the ring oscillator counter value with a factor, k, that is calibrated through spice simulations, in Equation 4.1.

$$\frac{V_{drop}}{V_{ideal}} = k \times \frac{ROC\_value_{drop}}{ROC\_value_{ideal}} \tag{4.1}$$

The ring oscillator based supply noise detector offers a purely digital design approach. There is no custom layout required. Every component can be synthesized and auto placed and routed. The detector can be implemented as a hard macro. No change of the RTL design is required to insert and operate the circuit. After the operation of the detector is done it can be turned off completely and it will not have any side effects on the original circuit.

It is compulsory for the detector to have the smallest possible area, allowing for numerous test points. This has motivated the use of a ripple-carry adder in the ring oscillator counter. Though the ripple-carry adder is the smallest possible adder, it has an obvious drawback of long delay, especially as the counter gets wider. To make the ring oscillator counter work properly, more stages of NAND2 gates are required in the ring oscillator to reduce the frequency of the clock signal. The extra NAND2 gates diminish the area saved by using a smaller adder. From the result of

a trial design in the predicted 45nm technology cell library[60] provided by NCSU and OSU, a 59-stage NAND2 ring oscillator is required for an 11-bit counter with a ripple-carry adder inside. The total gate area for each detector is around 275 NAND2 gates area.

4.2 Proposed detector scheme

The proposed detector scheme consists of the sensors and control unit, as illustrated in Figure 4.3. The ring oscillator functions as the sensor. The ring oscillator is the only segment that is affected by the supply voltage variation in this scheme. Placement of the ring oscillator depends on the power supply noise estimation contour. If q locations are in the interest of detection, total q ring-oscillators are needed while sharing only one control unit. The control unit assigns one ring oscillator to be operated, determines the timing window of detection, detects the frequency variation of the ring oscillator, and evaluates the voltage drop. The location of the control unit is flexible as it is not sensitive to supply-voltage variations.

Analyzing measurement results represented as small signal voltage or current differences on-chip can be expensive. To circumvent this expense, this detector measures the voltage drop as a function of rising edges of the signal produced by the ring oscillator. In other words, the ring oscillator converts the supply voltage variation into observable information, i.e. frequency variation. The percentage of voltage drop due to chip activity is represented by the ratio of the ROC's value measured with voltage drop to the ROC's value of an inactive chip. The division can be easily implemented on-chip. The actual voltage drop levels correlate to certain

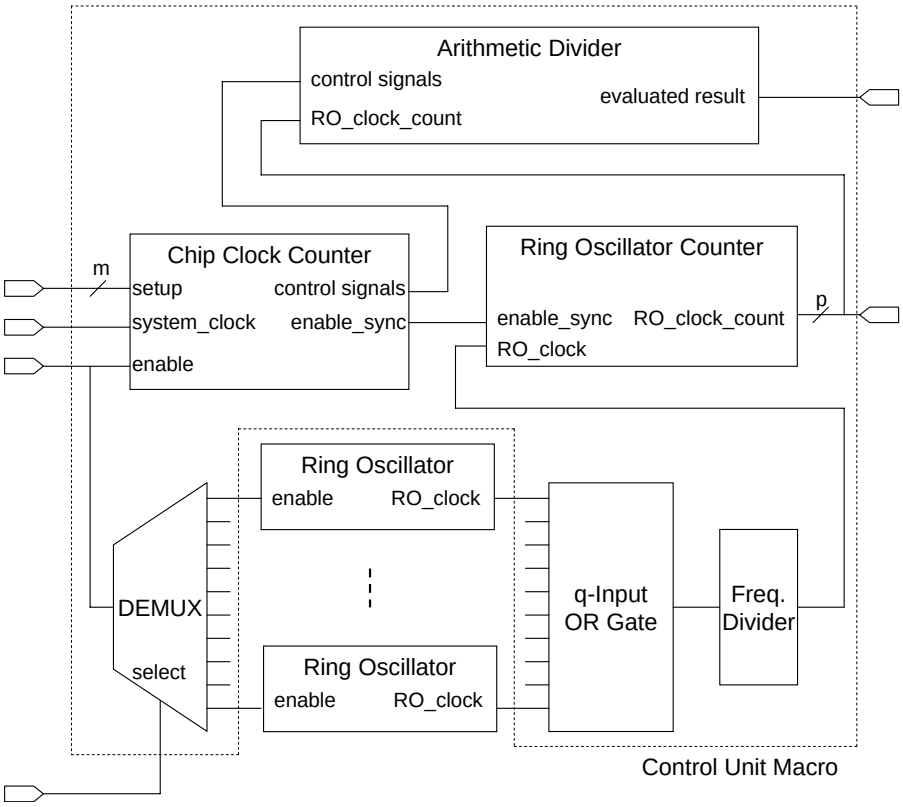


Figure 4.3: The supply noise detector shared by multiple ring oscillators

percentage values determined by running HSPICE simulation in advance.

The functionality of each component is explained below.

4.2.1 Control unit

The control unit includes a chip clock counter, a 1-to-q de-multiplexer, a q-input OR gate, a ring oscillator counter, and an arithmetic divider. All detectors integrated at selected test points share the same control unit; hence, the area cost of each additional detector will be approximately the size of the oscillator and the

area overhead in the OR gate and the de-multiplexer. In the conventional detector scheme, the ROC uses a ripple-carry adder to save area. A slower adder requires a longer ring oscillator with high area consumption. Since the control unit is shared between each ring oscillator, the critical path delay of the ROC can be reduced by using a fast adder without concern for the area. This allows for reduction in the length of the ring oscillators resulting in a smaller overall area. Since only one ring oscillator will be enabled at a time, an OR gate can be used rather than a multiplexer to capture the clock signals from the ring oscillators. The total detection time will be increased if the detectors are operated serially.

An arithmetic divider is placed within the control unit in the scheme to process the result producing the final figure for voltage drop on-chip. The divider takes the ROC value without (or less) voltage drop as the divisor and the ROC value with voltage drop as the dividend. The quotient of this division is the evaluated result of the average voltage drop within the detecting window.

4.2.2 Ring oscillator and frequency divider

Adding more stages of NAND2 gates seems like a naïve way to achieve a longer period. In this design, a D flip-flop divides the clock signal enabling us to double the period directly with the cost of one flop, as Figure 4.4 illustrates. The best combination of the number of NAND2 gates, n, and the number of frequency dividers may vary depending on the technology. This detector uses eleven NAND2 gates and one frequency divider to obtain the necessary clock period. By placing the frequency divider at the end of the OR gate, all oscillators share the same divider

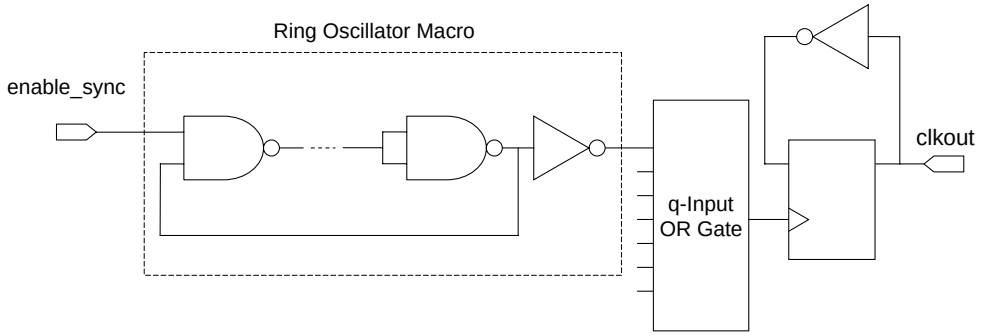


Figure 4.4: Ring oscillator and frequency divider

enabling us to further minimize the area.

To prevent the output load from affecting the frequency of the oscillator and to facilitate inserting the ring oscillator as a hard macro, an inverter is placed at the end of the oscillator. Sharing the control unit between multiple ring oscillators results in varying distances, and in some cases long distances, between oscillators and the control unit. As a result, the interconnect RC and interconnect delay for the path between each oscillator and control unit becomes hard to predict. An inverter is placed on the path back to the control unit to isolate the oscillator from the interconnect RC and to protect the oscillator frequency from being affected. The varying interconnect delay between the oscillators and the CCC may cause time offset, but it will not affect the width of the detecting window. The window width is of importance but the time offset does not affect the measured static voltage drop.

4.3 Implementation and simulation results

This detector scheme is implemented with a 7-bit chip clock counter and an 11-bit ring oscillator counter in the control unit. Therefore, the detecting window is a maximum of 127 clock periods, and it can count up to 2023 ring oscillator edges. There are a total of 64 ring oscillators; therefore it requires a 64-output demultiplexer and one 64-input OR gate. To calculate the final result, it uses an 11-bit sequential non-storing divider. Each division takes eleven cycles to finish. The total area of the 64 detectors, excluding the divider, is equivalent to 1161 NAND2 gates. The area of the divider is equivalent to 587 NAND2 gates. A previously published technique [43] would require a total area equivalent to 17984 NAND2 gates in order to insert 64 detectors. This is 15 times bigger than the proposed scheme. The area comparison for the different number of detectors inserted between the two schemes is shown in Figure 4.5.

In the experiment, the detector scheme with 64 ring oscillators is inserted into a test circuit, as shown in Figure 4.6. The test circuit includes four high speed FFT cores. The total gate count is 399956, and the core dimension of this circuit is 810 $\times$ 810 μm^2. The control unit of the detector is the box at the center of the design, and each ring oscillator is the highlighted dot in the figure. The dimension of the control unit and of each oscillator is 42 $\times$ 42 μm^2 and 4.56 x 4.94 μm^2 respectively.

Supply voltage, temperature, and process variation directly affect the frequency of the ring oscillator. To mimic the simulation of a real operating environment, Monte Carlo simulation is performed in HSPICE to verify the design. The

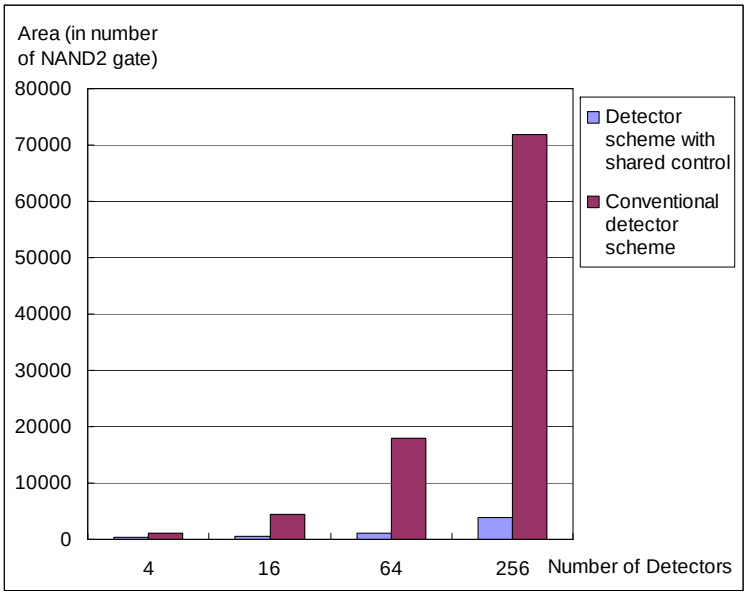


Figure 4.5: Area comparison

parasitic RC are first extracted from the post layout netlist of the ring oscillator. To account for process variations, 100 netlists are formed with different values for the channel length and the threshold voltage of the transistors, acquired from a normal distribution random number generator. The intra-die variation is neglected within the ring oscillator due to the small area the detector spans. The working temperature is set to values obtained from a uniform distribution random number generator in the range between 25°C and 100°C for those 100 netlists.

To calibrate the result, the supply voltage is controlled at 17 different voltage levels from the ideal of 0% to an 8% voltage drop with a 0.5% step between each level. The value of the supply voltage is also randomized by using the normal distribution random number generator, keeping the mean value of the voltage

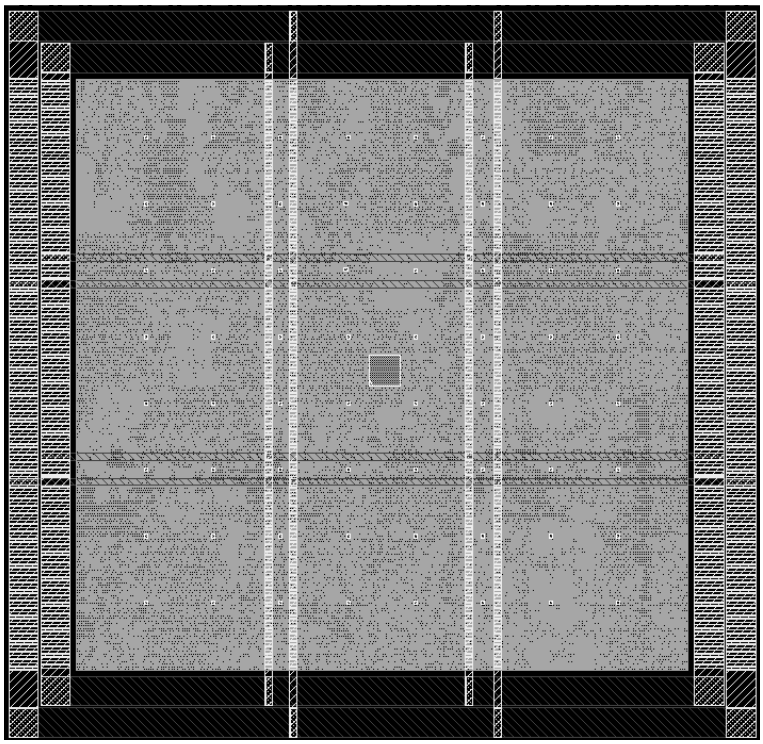


Figure 4.6: Detector scheme inserted into a test circuit

level at the expected level. The simulations of these 17 voltage levels are performed for all of the random netlists for the proposed scheme, as well as for the conventional scheme. The mean and standard deviations of the ROC value reduced ratio $\frac{ROC\_value_{with\_voltage\_drop}}{ROC\_value_{with\_ideal\_vdd}}$ are shown in Table 4.1.

Table 4.1 shows that the reduction in the ring oscillator frequency is proportional to the decrease of the voltage drop. The mapping factor, k, and the standard deviation for both designs are similar. Therefore, it can be concluded that there is no accuracy lost due to the shorter length of the ring oscillator. Assume that the error is within a three sigma range, the accuracy will be within $\pm$ 7.6 mV, while the voltage drop is between 4% and 6%. The 11-bit divider is wide enough so that the error caused by the divider can be ignored.

The average current consumption of operating each detector is only 1.1mA. Since only one oscillator would be operated at a time, the detector would not contribute considerable supply noise to the original circuit.

4.4 Limitation and discussion

From simulation result, though this detector can detect the voltage drop with fine voltage resolution, it is able to capture only low frequency supply noise. There is an essential tradeoff between the voltage resolution and the time resolution within the ring oscillator based detector. To achieve a higher time resolution, the detection window can be set at a shorter period with the cost of some accuracy lost.

Another limitation of this detector is the increased testing time. Only one

Table 4.1: Comparison of simulation results

	RO with 11 NAND2 Gates		RO with 59 NAND2 Gates	
V_{dd} Drop	ROC Value Reduced Ratio	Standard Deviation	ROC Value Reduced Ratio	Standard Deviation
0.5%	0.72%	0.08%	0.69%	0.11%
1%	1.39%	0.09%	1.39%	0.12%
1.5%	2.08%	0.08%	2.08%	0.12%
2%	2.77%	0.11%	2.79%	0.11%
2.5%	3.47%	0.11%	3.48%	0.13%
3%	4.18%	0.13%	4.18%	0.15%
3.5%	4.89%	0.14%	4.89%	0.17%
4%	5.59%	0.16%	5.60%	0.17%
4.5%	6.31%	0.18%	6.32%	0.21%
5%	7.02%	0.19%	7.03%	0.22%
5.5%	7.76%	0.22%	7.77%	0.22%
6%	8.49%	0.23%	8.49%	0.22%
6.5%	9.21%	0.25%	9.23%	0.25%
7%	9.96%	0.26%	9.97%	0.27%
7.5%	10.68%	0.28%	10.71%	0.27%
8%	11.44%	0.29%	11.46%	0.31%

detector can be operated at a time, since the area reduction is achieved by sharing the control unit for all of the detectors. Therefore, unavoidably the total detection time may increase. However, this detector significantly reduces the area cost. For the purpose of enormous detection location, this detector is still attractive.

One other limitation of this detector is the requirement of the calibration. Calibration is required to assure accuracy, since the process variation may differ from one detector to another, and the temperature may vary from time to time. Idle instruction is needed during the calibration to provide a stable voltage source. Therefore, it is not suitable for providing real-time alerts.

4.5 Summary

This chapter has presented an area efficient static supply noise detector/evaluator circuit capable of operating independently of any off-chip components. This detector scheme provides a simple, low-cost, and practical method to detect and to evaluate the static supply noise on-chip. This purely digital scheme can be inserted into any design as a hard macro to reduce the design complexity. The area is minimized by reducing the length of the ring oscillator and by sharing the control unit between all ring oscillators. In the detector scheme with 64 embedded detectors, this design has an area 15 times smaller than a conventional design. The simulation result shows that there is no accuracy lost while the area is significantly reduced.

In the next chapter, another on-chip power supply noise detector will be presented. This detector is robust against process and temperature variations. Therefore, it does not require calibration before measurement, which is required in the

detector presented in this chapter. Moreover, the time resolution of the detectable noise is also improved in the detector presented in the next chapter.

Chapter 5

An on-chip self-calibrating voltage uncertainty detector

The last chapter introduced an area-efficient power supply noise detector, which significantly reduces area consumption. However, it is similar to most of the other previous on-chip detectors in that it needs calibration to obtain accurate detection results. As a result, the application of that detector is limited. This chapter presents a novel on-chip detector scheme, SCOUT, which stands for **S**elf-**C**alibrating v**O**ltage **U**ncertainty de**T**ector. The SCOUT circuit is robust against process and temperature variations. In other words, this detector is able to calibrate itself and to provide consist measurement results regardless of process variation and ambient temperature changes. Furthermore, the SCOUT circuit is able to continuously monitors supply noise (not a single shot detection) and obtain the detection results in an absolute value (not only an undershoot or overshoot).

5.1 Detector design

The architecture of the SCOUT circuit consists of three major parts as shown in Figure 5.1. The on-chip reference voltage generator provides a constant voltage source to the voltage detector to be used as a reference voltage. The voltage detec-

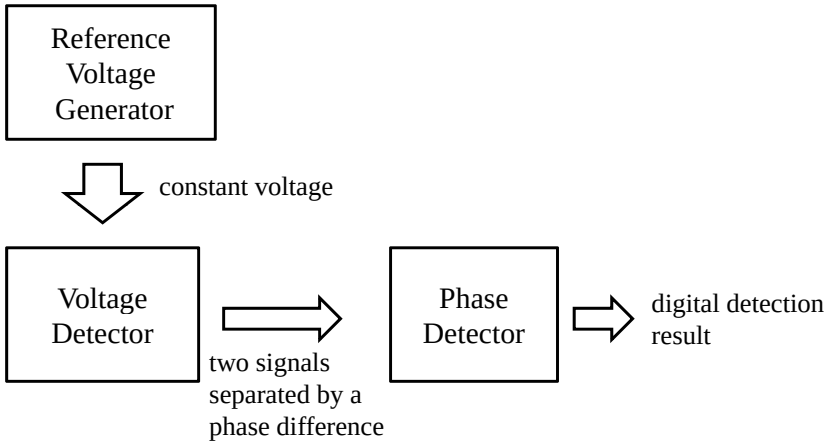


Figure 5.1: Overall block diagram

tor continuously generates two signals with a phase difference proportional to the voltage difference between the reference voltage and the local supply that is seen on the rail. Therefore, power supply noise can be determined by measuring the phase difference with the phase detector placed at the end. The detection results are digital signals and can be obtained on-chip without any off-chip processing or external test equipment. Each of the three blocks will be explained in more detail in the following subsections.

5.1.1 Voltage detector

The voltage detector is comprised of two identical delay lines as shown in Figure 5.2. Each delay line contains a two-input NAND gate and a series of inverters, $INV_{regular}$. Each $INV_{regular}$ is followed by a smaller inverter, INV_{tail}, to fix the output load of the $INV_{regular}$ and to provide the layout uniformity. The reason-

ing behind this will be explained within Section 5.1.2. The reference delay line (RDL) is supplied with a constant voltage, VDD_{clean}, generated by the reference voltage generator. The varied delay line (VDL) is supplied with the local power rail, VDD_{local}. The reset signal stops the activity of both delay lines when the detector is not in use. After the reset signal is de-asserted, the RDL behaves as a ring oscillator. The VDL is triggered by the switch signal which is an output signal from the RDL.

As the two delay lines are supplied by different voltage levels, a phase difference appears between the two signals, RDL_out and VDL_out as illustrated in Figure 5.3. This phase difference can be used to identify the average VDD_{local} within a period of the RDL. This is because the path delays of the RDL and VDL are determined by the average voltage within a RDL period and a VDL period respectively [52]. As a result, the delay variation ratio, $(T_{VDL} - T_{RDL})/T_{RDL}$, of the delay line is proportional to the voltage variation ratio, $(V_{VDL} - V_{RDL})/V_{RDL}$. As the RDL continues to oscillate, it triggers the VDL, thus power supply noise can be continuously monitored for as long as the reset signal is de-asserted.

A single VDL is not enough to detect the voltage variation, since the VDL is affected by both process and temperature variations. Dynamic calibration must be performed to cancel effects of these variations. Therefore, a RDL is required to provide a reference from which to obtain the delay variation ratio for self-calibration purposes.

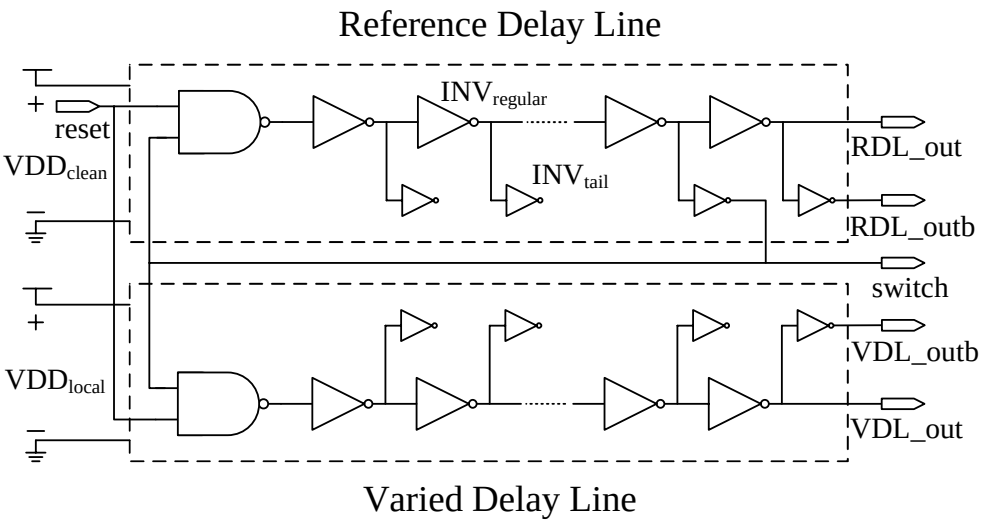


Figure 5.2: Schematic of the voltage detector

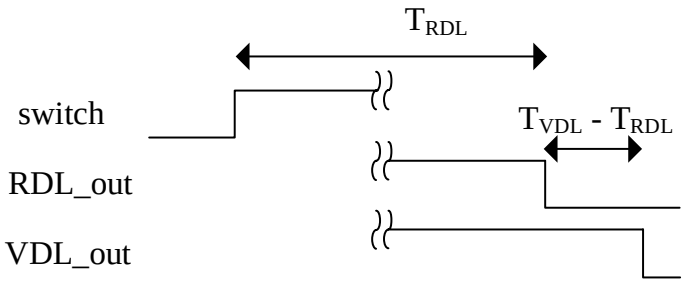


Figure 5.3: phase difference between RDL_out and VDL_out

5.1.2 Phase detector

The purpose of the phase detector is to measure the phase difference generated by the voltage detector. The phase detector is also implemented by two identical delay lines, which consist of the same delay elements as the RDL and the VDL. The circuit implementation is illustrated in Figure 5.4. The upper delay line takes the signal RDL_out as its input and the lower delay line takes the signal VDL_out as its input. The two delay lines are both supplied by the same local power rail. As a result, the two delay lines within the phase detector do not introduce additional phase difference besides the original phase difference between the RDL_out and the VDL_out signals.

A typical master-slave flip-flop is inserted after the INV_{tail} in every other stage of the delay lines. The switch signal is connected to a pulse generator. Each toggling of the switch signal generates a pulse triggering the flip-flops to capture the phase difference between the two delay lines. An XOR gate compares the output signals of the two flip-flops at the same stage. If the polarity is opposite, the XOR gate indicates "1"; otherwise, it indicates "0". The amount of the phase difference can be determined by counting the number of "1"s for all of the XOR gates.

The RDL_outb and the VDL_outb signals are connected to two pulse generators followed by two flip-flops. These two flip-flops indicate that the VDL_out signal is either faster or slower than the RDL_out signal, which implies that the local VDD is either higher or lower than the reference voltage. An example timing diagram is illustrated in Figure 5.5. From the detection results in Figure 5.5, power supply noise causes phase differences in two stages and the local VDD is lower than

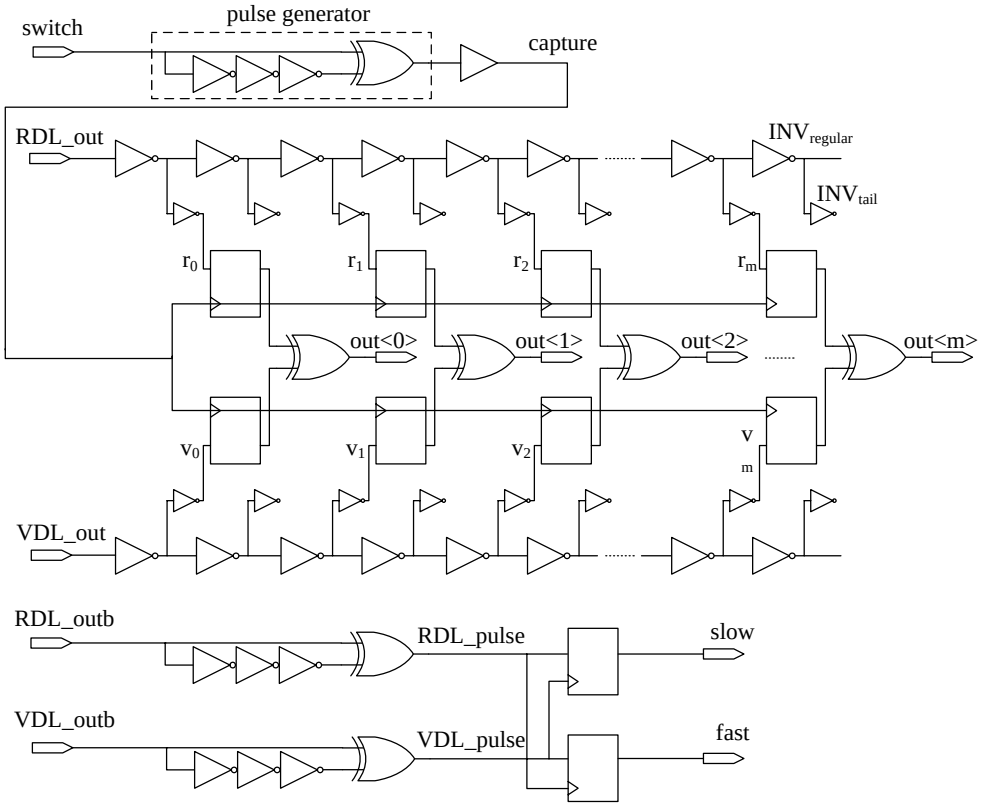


Figure 5.4: Schematic of the phase detector

the reference voltage.

The detection results can be expressed as in Equation 5.1, in which n indicates the number of "1"s contained within the XOR gates and *slow* and *fast* are the binary output of the "slow" and "fast" flip-flops.

$$Result = n * (fast - slow) \tag{5.1}$$

A lookup table of the detection results according to the local power supply noise is built through the transient analysis based on the post-layout netlist. Thus, a de-

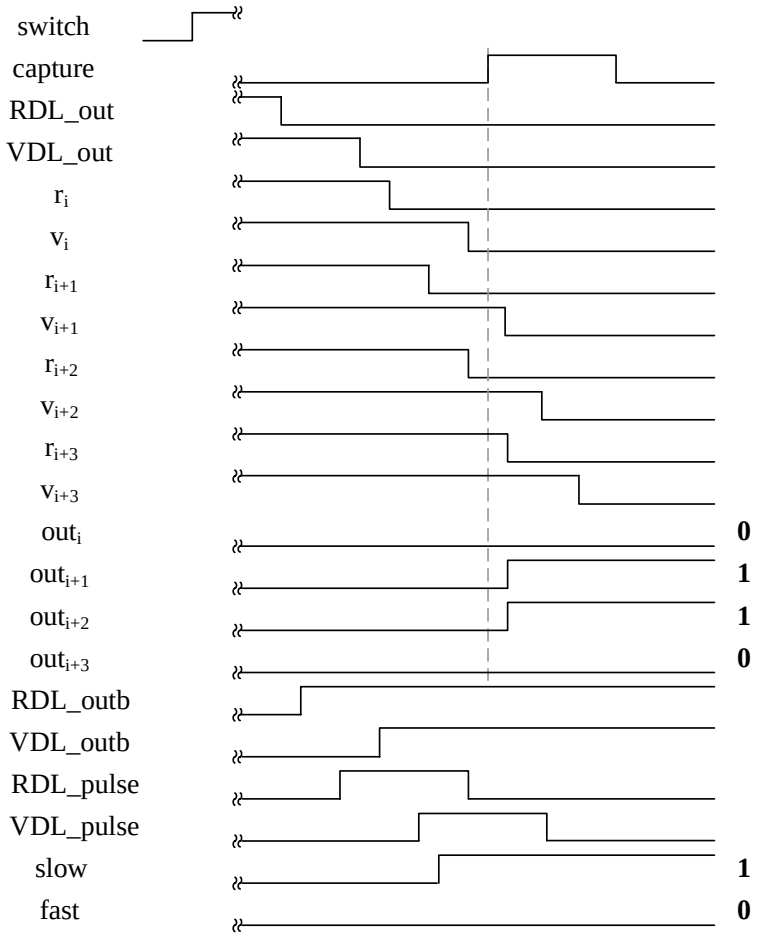


Figure 5.5: Example timing diagram of phase detector

tection result can be interpreted as an absolute value of the measured power supply noise.

It may be more clear now why there is a smaller inverter INV_{tail} following the $INV_{regular}$ in each stage of the delay line. This INV_{tail} is to make the delay of each delay element within both the voltage detector and the phase detector the same, because the phase detector should not introduce additional phase differences. The INV_{tail} is used to fix the load on each $INV_{regular}$ within the delay lines. An alternative would be to directly insert flip-flops after the $INV_{regular}$ without the flops being buffered by an INV_{tail} within each stage of the voltage detector and the phase detector. However, the area overhead would be much larger.

5.1.3 Reference voltage generator

The reference voltage generator provides a regulated power supply voltage for the RDL within the voltage detector with necessary DC output current. The reference voltage generator consists of a bandgap voltage reference [61] and a low-drop-out voltage regulator (LDO). The bandgap voltage reference provides a constant voltage for the LDO regardless of the variations of power supply, temperature, or process. The LDO consists of a Miller-compensated 2-stage amplifier, feedback resistors, and an NMOS by-pass capacitance. The NMOS by-pass capacitance surrounds the RDL evenly to provide a low ac impedance path for instantaneous current so that voltage ripple due to the activities of the delay chain is negligible. If there are other stable reference voltage sources, such as dedicated pins for external power supply, the reference voltage generator may not be required.

5.2 Self-calibration

The SCOUT circuit is designed to operate without requiring calibration. This is achieved by using one additional reference delay line (RDL) except the VDL within the voltage detector to eliminate the inter-die process variation. If the RDL and the VDL are placed close enough, the temperature impact on both delay lines is the same, and the two delay lines should have similar intra-die process variation. Moreover, careful layout techniques, such as symmetric layout and interdigitate the delay lines, reduce the systematic process variation. The random process variation will tend to be averaged out within the delay lines, since there are multiple inverters within the delay lines. As long as the RDL and the VDL have the same process and temperature variations, the voltage impact on the delay variation is similar in any situation. This is verified by simulating a ring oscillator in HSPICE and examining the period variation of the ring oscillator according to the voltage variation. Simulations were made when the circuit was in extreme process corners, {FF, FNSP, SNFP, and SS}, and at extreme temperatures {0 °C and 100 °C}, as shown in Figure 5.6. Simulation results reveal that the trends of $\triangle T_{VDL}/\triangle VDD$ differ only slightly between the circuits located at different process or temperature corners.

Using identical delay elements to implement the phase detector also achieves self-calibration. A heterogeneous implementation of the phase detector may lose accuracy under the impact of process and temperature variations, thus requiring calibration. A homogeneous implementation of the voltage detector and the phase detector is able to keep the process and temperature impacts the same. By taking this approach, the voltage detector and the phase detector are able to calibrate each

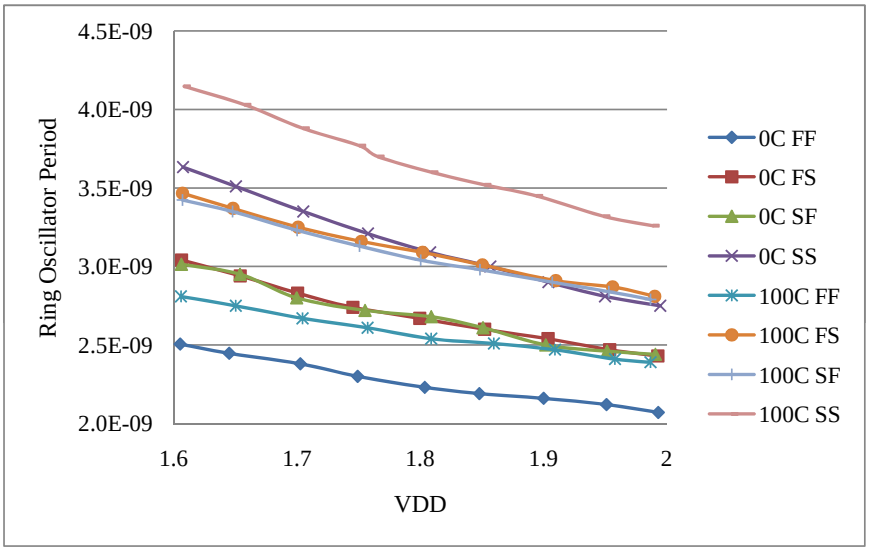
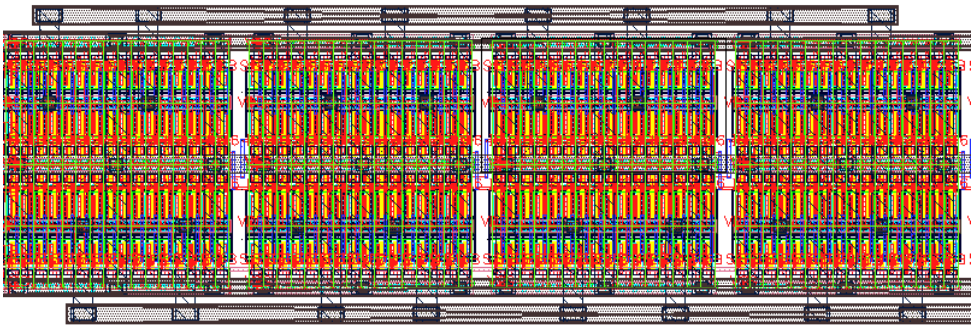


Figure 5.6: Ring oscillator periods for different VDD values at different temperatures and process corners

other automatically.

Minor detection errors may still appear because of process and temperature variations, even though the SCOUT circuit is designed to be self-calibrated against these variations. In a situation in which a strict requirement on the detection error is needed, e.g. validating an EDA tool, performing a one-time calibration can further reduce the detection error. The one-time calibration is achieved by characterizing the SCOUT circuit after the chip is fabricated. The voltage threshold of this detector is redefined according to the characterization results. Therefore, the detection error due to the process variation would be effectively eliminated through this one-time calibration. In addition, the dynamic run-time calibration is still not required, since the detection error caused by temperature variation is ignorable. If the requirement



RDL_part1	VDL_part2	RDL_part3	VDL_part4
VDL_part1	RDL_part2	VDL_part3	RDL_part4

Figure 5.7: Interleaving RDL and VDL reduces the impact of systematic intra-die process variation

for detection error is moderate, this one-time calibration would not be necessary.

5.3 Layout of delay lines

As mentioned in the previous section, the delay lines within the voltage detector is implemented with careful layout. First, the RDL and the VDL are interleaved with each other as illustrated in Figure 5.7. Therefore the impact of systematic process variation can be minimized.

The RDL and the VDL also have an exact symmetric layout as illustrated in Figure 5.8. The $INV_{regular}$ of both delay lines is placed in between the INV_{tail} of

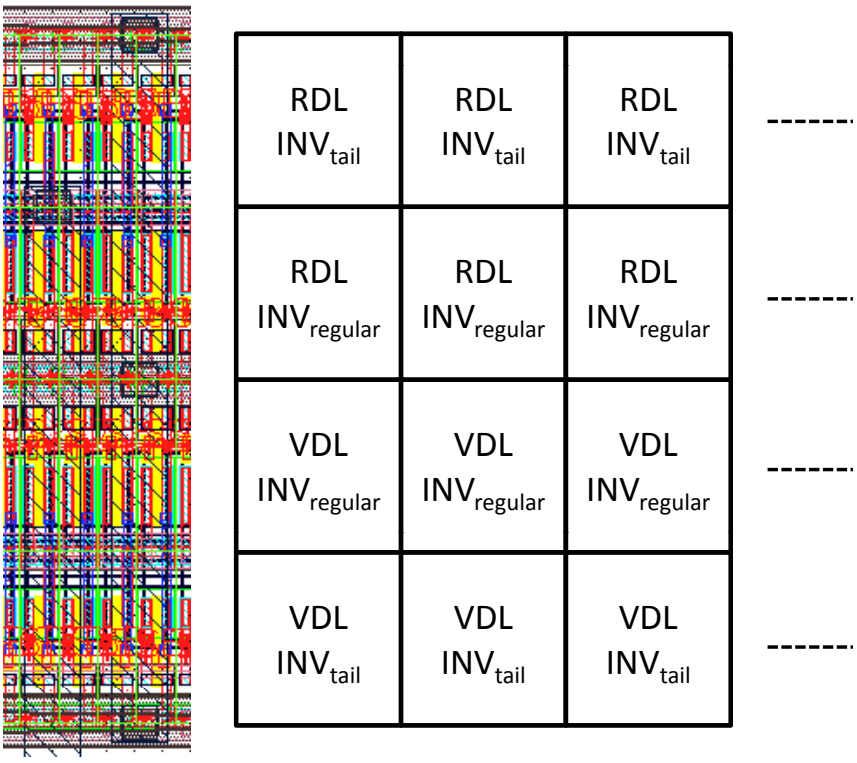


Figure 5.8: Symmetric layout of the RDL and the VDL

both delay lines. Therefore, the surrounding layout of each $INV_{regular}$ within both delay lines is the same. Hence the intra-die process variation can also be reduced.

5.4 Design considerations and limitations

There is a design tradeoff between the detectable voltage resolution and the time resolution of the SCOUT circuit. This design tradeoff is also a concern for all other power supply noise detectors which use delay lines or ring oscillators for detection as discussed in the previous chapter.

The principle of the SCOUT circuit is to detect the voltage variation by detecting the delay variation on the delay lines. The delay variation becomes more significant when the delay lines are longer. The time resolution is determined by the period of the RDL within the voltage detector. Therefore, using longer delay lines within the voltage detector achieves a finer voltage resolution but a looser time resolution. Deciding the length of the delay lines depends on both of the voltage resolution and time resolution in interest and may vary according to different applications.

The dynamic range of the detectable voltage is determined by the delay line length within the phase detector. Determining the length of the delay line should consider both the area available budget and the voltage range of interest.

Within the phase detector, flip-flops are used to capture the phase differences between the RDL_out and the VDL_out signals. In this implementation, these flip-flops are inserted in every other stage of the delay lines. These flip-flops may also be inserted in every stage of the delay lines to achieve finer voltage resolution at the price of larger area. However, the detection error represented in the least significant bit (LSB) becomes larger due to the fact that the detection error represented as voltage remains the same but the voltage resolution becomes finer. As a result, the benefit of inserting flip-flops in every stage is not an absolute, and further analysis is required for other implementations.

Although the voltage detector and the phase detector are placed next to the reference voltage generator in this implementation, it is not required in other implementations. The voltage detector and the phase detector should be inserted at the

local detecting point, but the reference voltage generator can be placed separately. The voltage variation caused by the distribution network of the clean VDD can be ignored. This is because the average current consumption of the RDL, from simulation result, is only 0.38 mA, and the N-type by-pass capacitance is inserted next to the RDL. In addition, when there is a need for detecting supply noise in multiple locations, only the voltage detector and the phase detector are required to be duplicated and inserted in the locations of interest. The reference voltage generator is able to be shared by all of the voltage detectors. However, the requirement of the additional power network for the reference voltage will become an additional design cost.

In order to perform self-calibration, one limitation of the SCOUT circuit is that the time resolution may vary. As mentioned previously, the time resolution is determined by the period of the RDL. The RDL period may vary when process and temperature variations appear. There may be a need for a supplemental circuit, if the timing resolution is necessary information.

5.5 Implementation and simulation results

A SCOUT circuit was implemented in the TSMC $0.18\mu m$ technology. Both the RDL and the VDL within the voltage detector consist of 64 delay element stages. The phase detector consists of two 16-stage delay lines, and each delay line is connected to eight master-slave flip-flops. The post-layout netlist of the SCOUT circuit is extracted and simulated with HSPICE. For the purpose of reducing the simulation time, the reference voltage generator is replaced by a DC

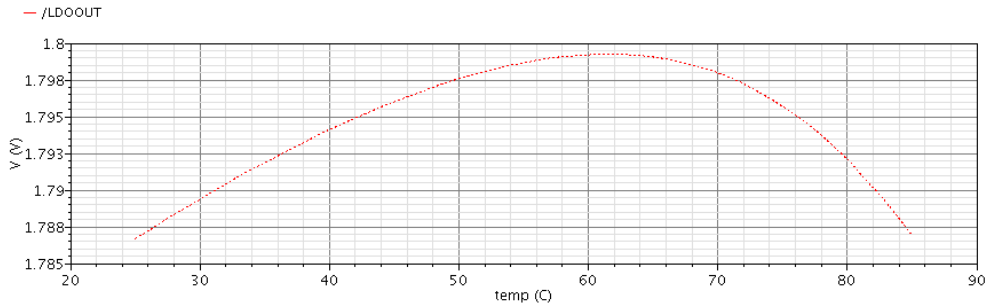


Figure 5.9: Reference voltage variation with respect to temperature variation

voltage source. Temperature variation is the major source varying the reference voltage on the bandgap reference, and it needs to be characterized. Assume that the operating temperature of the circuit ranges between 25 and 85 °C. The reference voltage varies between 1.787V and 1.799V as shown in Figure 5.9. According to Figure 5.9, the DC value of the reference voltage source is determined depending on the assigned temperature. The simulations for verifying the voltage resolution, time resolution, and current consumption are described in the following sections.

5.5.1 Voltage resolution

5.5.1.1 Corner-based simulations

The corner-based simulations are performed first to characterize the detection results at the output and to ensure the maximum error in those extreme corners. The circuit was simulated at 25 different combinations of five process corners (FF, FNSP, SNFP, SS, and TT) and five temperatures (25, 43, 61, 73, and 85 °C). The DC value of the reference voltage are assigned to five different values (1.787V, 1.795V, 1.799V, 1.797V, and 1.787V) according to different temperatures as shown in Fig-

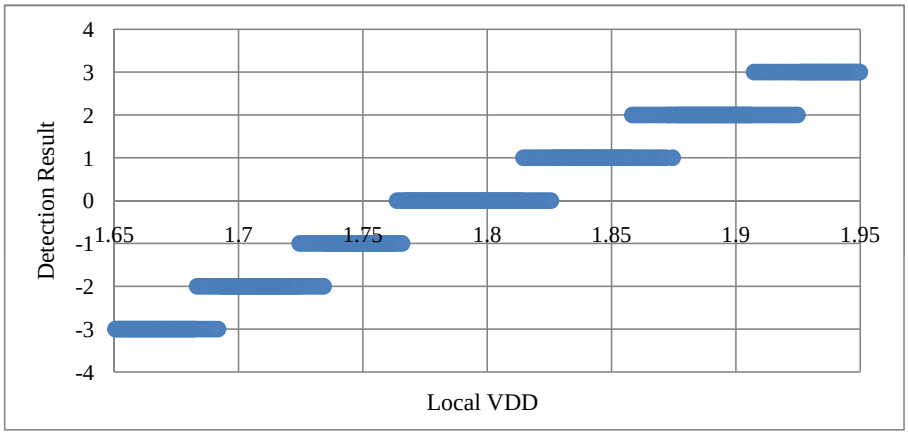


Figure 5.10: Detection result when circuit is in the SS corner at 85 °C

ure 5.9. The local VDD sweeps across a range, 1.8±0.15V. The simulation results are calculated using Equation 5.1 and are illustrated in Figure 5.10, for the case of the SS corner with a temperature of 85 °C.

The results for all 25 combinations are summarized in Table 5.1. From this table, one can see that this implementation effectively detects power supply noise without any calibration. The detection result are represented by six output levels while the local VDD is within 1.8±0.15V range, since there are five voltage thresholds.

The detected voltage resolution (the step between two voltage thresholds) is less than 49mV when there is negative supply noise (local VDD $<$ 1.8V) and 62mV when there is positive supply noise (local VDD $>$ 1.8V). The detection error is smaller when there is less power supply noise. The maximum error is 28mV (0.56 LSB) when there is a 118mV negative supply noise and 41mV (0.67 LSB)

Table 5.1: Maximum detection error at 25 combinations of corners {FF, FNSP, SPFN, SS, and TT} and temperatures {25, 43, 61, 73, and 85 °C}

Voltage Threshold	Between Level	Max Error	
		Voltage	LSB
1.675V	-3∼-2	0.028V	0.56
1.724V	-2∼-1	0.021V	0.52
1.764V	-1∼0	0.014V	0.36
1.839V	0∼1	0.026V	0.42
1.901V	1∼2	0.041V	0.67

when there is a 110mV positive supply noise. The LSB is defined as the voltage step between the threshold voltage and adjacent threshold voltages. Therefore, the LSB may vary according to the local VDD, since the steps between the thresholds are slightly different.

To examine the effectiveness of the one-time calibration, the SCOUT circuit is simulated at a specific process corner but varying the temperatures across 25, 43, 61, 73, and 85 °C. The voltage thresholds are redefined for each circuit at different corners. The detection error from the simulation results of the five extreme process corners is listed in Table 5.2. Notice that the maximum detection error is reduced to 12mV (0.26 LSB) for negative supply noise and 25mV (0.35 LSB) for positive supply noise. These results also demonstrate that the detection error can be reduced by using a one-time calibration, when a strict requirement on detection error is needed. Note that dynamic run-time calibration is still not needed.

Table 5.2: Simulation results across temperatures {25, 43, 61, 73, and 85 °C} for five process corners individually

Process Corner	Max Detection Error For Negative Noise		Max Detection Error For Positive Noise	
	Voltage	LSB	Voltage	LSB
FF	0.012V	0.26	0.025V	0.35
FNSP	0.009V	0.26	0.017V	0.30
SNFP	0.010V	0.24	0.019V	0.32
SS	0.009V	0.26	0.013V	0.28
TT	0.011V	0.29	0.017V	0.30

5.5.1.2 Monte Carlo simulations

Monte Carlo simulations were performed on 200 random netlists to verify how the maximum detection error may distribute among different circuits with random process, voltage, and temperature variations. The inter-die process variation is introduced by using the static SPICE model with different random seeds for each individual netlist. The random intra-die process variation is introduced by inserting random vt variation into each individual transistor. The random vt variation spans $\pm 2\sigma$ of the standard deviation on top of the inter-die variation. The temperature of each netlist is generated by a uniform random number generator and is within 25 °Cand 85 °C. The DC value of the reference voltage depends on the simulation temperature and is assigned according to Figure 5.9. The local VDD waveform is generated by a random number generator covering a voltage range between 1.8±0.15V.

The statistics of the simulation for the 200 random netlists are summarized

Table 5.3: Distribution of maximum detection error among 200 netlists with random process, voltage, and temperature variations

Voltage Threshold	Between Level	Max Detection Error	
		Mean Value	Std. Deviation
1.675V	-3∼-2	0.010V	0.006V
1.724V	-2∼-1	0.009V	0.004V
1.764V	-1∼0	0.006V	0.004V
1.839V	0∼1	0.013V	0.005V
1.901V	1∼2	0.022V	0.007V

in Table 5.3. The voltage thresholds were set according to Table 5.1. From Table 5.3, one can see that the mean value of the maximum detection error within these random netlists is quite small even without performing any calibration.

5.5.2 Time resolution

The variations of time resolution for the five process corners and five temperatures are listed in Table 5.4. The worst time resolution (at the SS corner and at 85 °C) is 3.7ns, which is usually less than or near the clock period for circuits implemented in $0.18\mu m$ technology. Therefore, the SCOUT circuit is able to provide useful information to debug delay faults.

5.5.3 Current consumption

The average current drawn from the local power rail during the operation of a SCOUT circuit is only about 2.4mA. Therefore, the SCOUT circuit does not

Table 5.4: Time resolution of detection results in different process corners and at different temperatures

Process	Temperature				
Corner	25 °C	43 °C	61 °C	73 °C	85 °C
FF	2.5ns	2.5ns	2.6ns	2.6ns	2.7ns
FNSP	2.9ns	3.0ns	3.0ns	3.1ns	3.2ns
SNFP	2.9ns	2.9ns	3.0ns	3.1ns	3.1ns
SS	3.4ns	3.4ns	3.5ns	3.6ns	3.7ns
TT	2.9ns	2.9ns	3.0ns	3.1ns	3.1ns

contribute to any significant power supply noise.

5.6 Chip measurement results

The SCOUT circuit is fabricated with TSMC $0.18\mu m$ technology. The die photo is shown in Figure 5.11. The dimension of the voltage detector and the phase detector is $178\mu m \times 90\mu m$. The dimension of the reference voltage generator is $520\mu m \times 380\mu m$. Besides the SCOUT circuitry, one performance monitor, a simple ring oscillator, is also implemented to monitor the speed of the fabricated chip. Five chips with different ring oscillator frequency are measured. The measurement is done under room temperature, and the local VDD is controlled by DC power supply. The results are summarized in Table 5.5

From Table 5.5, it can be found that the speed variation is roughly 10% between the fastest and the slowest chip. However, the behavior of the SCOUT detector is still consistent even without any calibration performed.

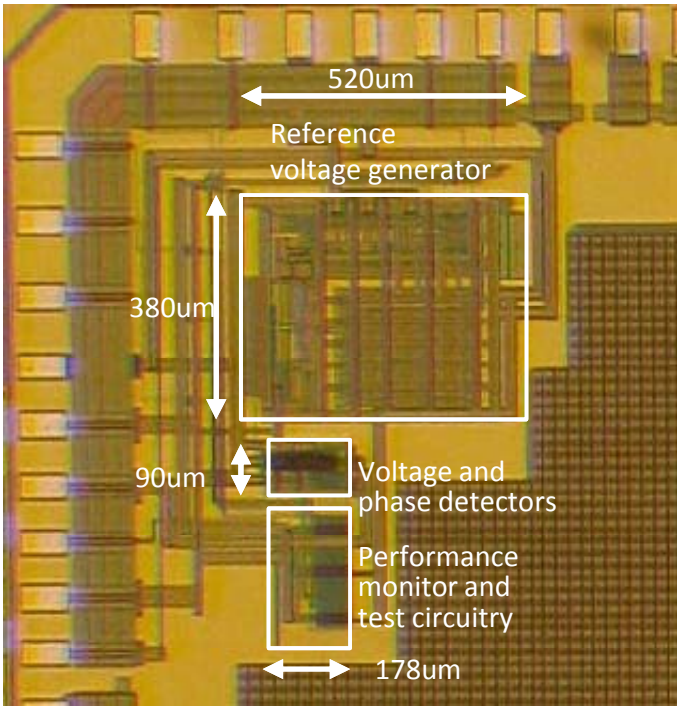


Figure 5.11: Die photo of the SCOUT detector

Table 5.5: Measurement results of five chips

	Voltage threshold between each level					Ring oscillator
	-3∼-2	-2∼-1	-1∼0	0∼1	1∼2	frequency
Chip1	1.668V	1.725V	1.765V	1.845V	1.893V	973KHz
Chip2	1.693V	1.745V	1.775V	1.845V	1.900V	971KHz
Chip3	1.683V	1.733V	1.780V	1.835V	1.895V	976KHz
Chip4	1.683V	1.730V	1.760V	1.840V	1.895V	1075KHz
Chip5	1.688V	1.730V	1.780V	1.835V	1.893V	1018KHz

5.7 Summary

This chapter presents the design of a novel on-chip power supply noise detector, SCOUT, with the following characteristics:

1. It performs self-calibration against process and temperature variations without the need of manual operation or external test equipment.
2. It obtains the result on chip without any off-chip processing.
3. It obtains a detection result in an absolute value (not an undershoot or overshoot).
4. It continuously monitors supply noise (not only a single shot detection).

The SCOUT circuit utilizes a voltage detector to detect the voltage difference between the local VDD and the reference voltage source and generates two signals with a phase difference. The phase difference is detected by a phase detector with a homogeneous implementation as the voltage detector. Since the SCOUT circuit is able to perform continuous detection without calibration, it provides the capability to detect power supply noise and to provide the real-time alert. In the next chapter, this SCOUT circuit will be utilized within a dynamic wakeup sequence control scheme as a real-time monitor. The next chapter also demonstrates how an on-chip detector can contribute to actively improve the design quality.

Chapter 6

Robust power gating reactivation by dynamic wakeup sequence throttling

The last chapter presents a self-calibrating power supply noise detector, which provides the capability to detect power supply noise and to provide a real-time alert. This chapter presents a new power gating reactivation scheme utilizing the on-chip detector to dynamically throttle the wakeup sequence according to the ambient voltage level. The overall power supply noise is thereby constrained beneath an established threshold even when the adjacent active circuit blocks induce an unexpectedly high voltage drop. The voltage drop mentioned in this chapter indicates the cycle-average voltage drop, which reflects the impact of supply noise on path delay as discussed in Chapter 1.

6.1 Power gating technique and related issues

As leakage current increases with technology advances, static power consumption has become comparable with dynamic power consumption. The power gating technique, or multi-threshold CMOS (MTCMOS), is recognized as one of the most effective techniques to reduce power leakage and has been broadly adopted in modern low power circuit design. The power gating technique uses a sleep tran-

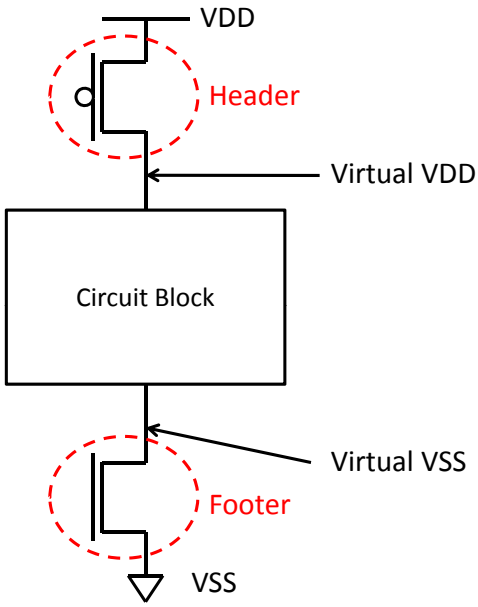


Figure 6.1: Typical power gating technique scheme

sistor to control the power and ground sources for the circuit blocks as shown in Figure 6.1. The sleep transistor provides virtual power and ground when the blocks are activated and cuts off the power and ground of the circuit blocks when the blocks are not in use. Though it has been demonstrated in Figure 6.1 that the circuit can be equipped at both the header and the footer, usually only one is required.

The IR drop caused by the *ON* resistances of the sleep transistors and the power supply noise caused by the rush current during the wakeup phase are the two major issues while designing the power gating schemes. The wakeup scheme proposed in this chapter targets the later issue. The voltage drop problem caused by the rush current is illustrated in Figure 6.2. The high rush current may cause the

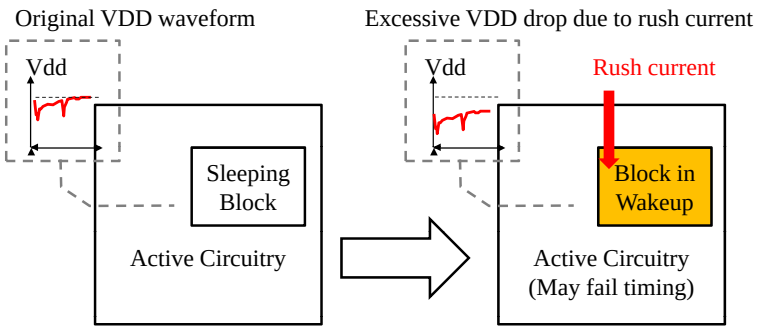


Figure 6.2: Excessive power supply noise due to the rush current

surrounding circuitry in normal operation mode to fail. Therefore, it is necessary to schedule the wakeup sequence properly to constrain the peak current and to avoid excessive supply noise.

The power supply noise seen on the local power rails during the wakeup phase consists of the voltage drop caused by the rush current, ΔV_{wakeup}, and the voltage drop induced by other active circuitry, ΔV_{active}. Therefore, ΔV_{active} must be considered when deciding the maximum tolerable ΔV_{wakeup} as a design constraint of the wakeup sequence. The design constraint can be written as $\Delta V_{wakeup} + \Delta V_{active} < \Delta V_{tolerable}$ as illustrated in Figure 6.3. However, if an unexpected circuit event occurs introducing an extreme ΔV_{active} during the wakeup sequence execution, the circuit may fail timing. Therefore, an extra voltage margin is required to protect the active circuitry from the unpredicted high ΔV_{active}.

Four common approaches can be applied to create the extra voltage margin ΔV_{margin} as shown in Figure 6.4:

1. Add ΔV_{margin} on top of the $\Delta V_{wakeup} + \Delta V_{active}$ by raising the VDD voltage

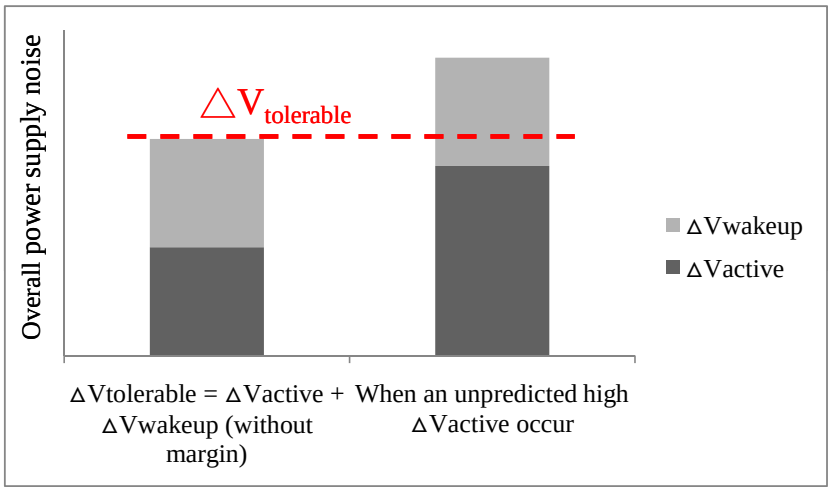


Figure 6.3: Circuit may fail when ΔV_{active} is greater than estimated value level.

2. Enhance the power distribution and create ΔV_{margin} by reducing both ΔV_{wakeup} and ΔV_{active}.

3. Constrain the ΔV_{wakeup} to be smaller to create ΔV_{margin}.

4. Constrain the ΔV_{active} to be smaller to create ΔV_{margin}.

All of these four methods can solve the problem of unpredicted high ΔV_{active}, but they also create new issues. Power consumption will increase while using the first method, which is not acceptable in low-power applications. Moreover, raising VDD may cause hold time violation, so min delay constraint need to be rechecked and new timing violations may occur. More area and routing resource will be consumed by the second method due to inserting more decoupling capacitors or widen-

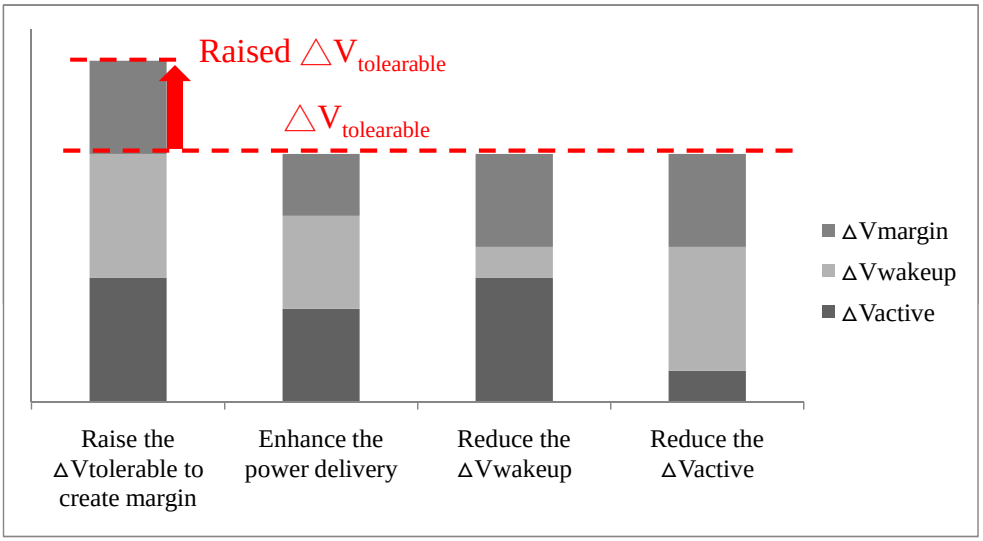


Figure 6.4: Four common approaches to add ΔV_{margin}

ing the power network. Moreover, increasing the width of the power net also increases the interconnect capacitance, which may slow down the circuit paths and increase power consumption as well. The third method extends the wakeup latency by constraining the rush current to a smaller value. This approach may cause some performance penalty, because the sleeping block needs more time to be woken up. The fourth method suppresses the activity within the active circuity, such as issuing an IDLE instruction during the execution of wakeup sequence, and creates voltage margin. This method may also create performance penalty, since the executing tasks are slowed down. All of these four solutions increase fixed design cost for the design, even though the extreme ΔV_{active} may happen rarely. Therefore, these methods do not provide an optimal solution.

The motivation of this novel wakeup scheme is to develop an ambient volt-

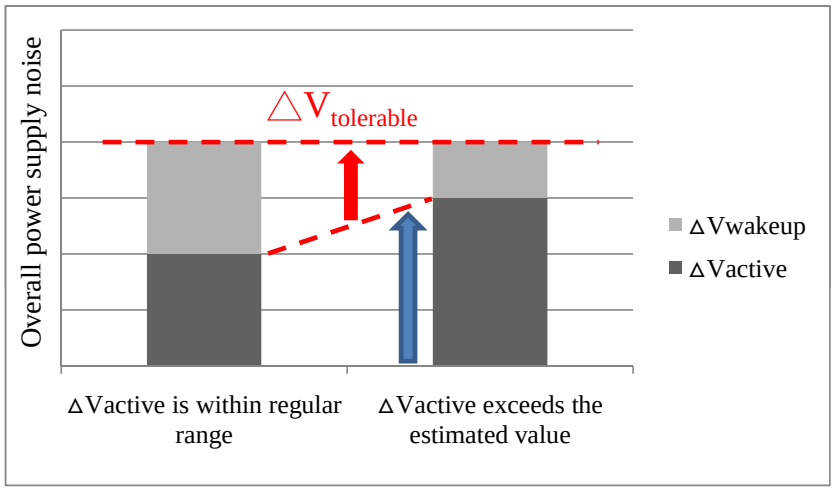


Figure 6.5: ΔV_{wakeup} is dynamically constrained according to the real-time ΔV_{active}

age aware dynamic wakeup throttling scheme. In this approach, the control unit follows the regular wakeup sequence when the ΔV_{active} is within the estimated range as illustrated in Figure 6.5. When a high voltage drop is detected, the control unit rolls the wakeup signal back and dynamically controls the wakeup sequence. Therefore, the problem of excessive ΔV_{active} can be efficiently solved by adding very few design resources.

However, in order to become robust against the unpredicted high ΔV_{active}, inevitably some pessimism need to be added into the dynamic wakeup throttling scheme. Therefore, the wakeup time may be extended in some circumstance. To reduce the impact of the pessimism on the wakeup time, a speedup mechanism is also added into the dynamic throttling scheme. The idea of the speedup mechanism is to utilize the voltage margin more efficiently when the $\Delta V_{active} + \Delta V_{wakeup}$ is lower than a certain threshold. This concept is illustrated in Figure 6.6. When there is

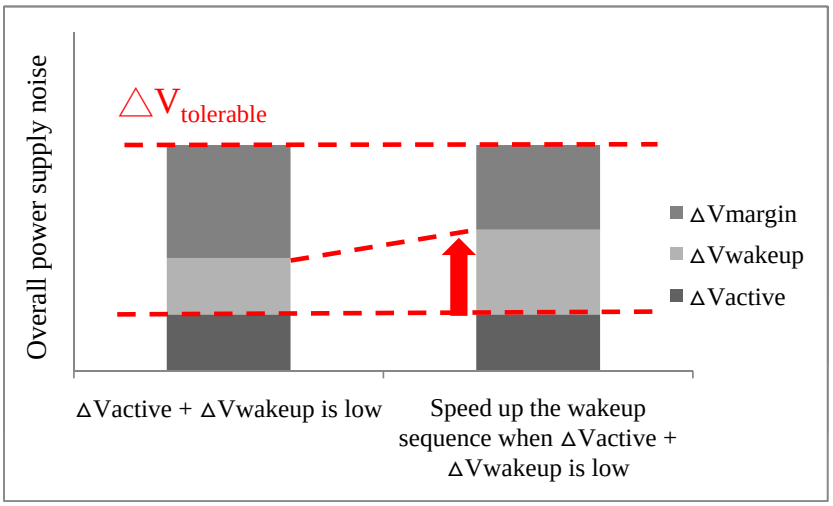


Figure 6.6: Speed up the wakeup sequence when $\Delta V_{active} + \Delta V_{wakeup}$ is low

enough voltage margin, the wakeup control unit takes advantage of this margin and increases the ΔV_{wakeup} by propagating the wakeup signal faster.

6.2 Dynamic reactivation throttling

The general idea of this dynamic wakeup scheme is illustrated in Figure 6.7. This implementation builds on the work of [47]. However, the proposed method theoretically could be adopted by any other wakeup scheme. In this implementation, the wakeup signal for each sleep transistor is delayed by a clock cycle, and the sleep transistor size is $\times 1.5$ larger for each stage. An on-chip power supply noise detector presented in the previous chapter is placed into the scheme to monitor the effective VDD (VDD - VSS) of the adjacent circuit blocks in real time. This detector asserts a SLOW_DOWN signal when it detects a voltage drop exceeding the

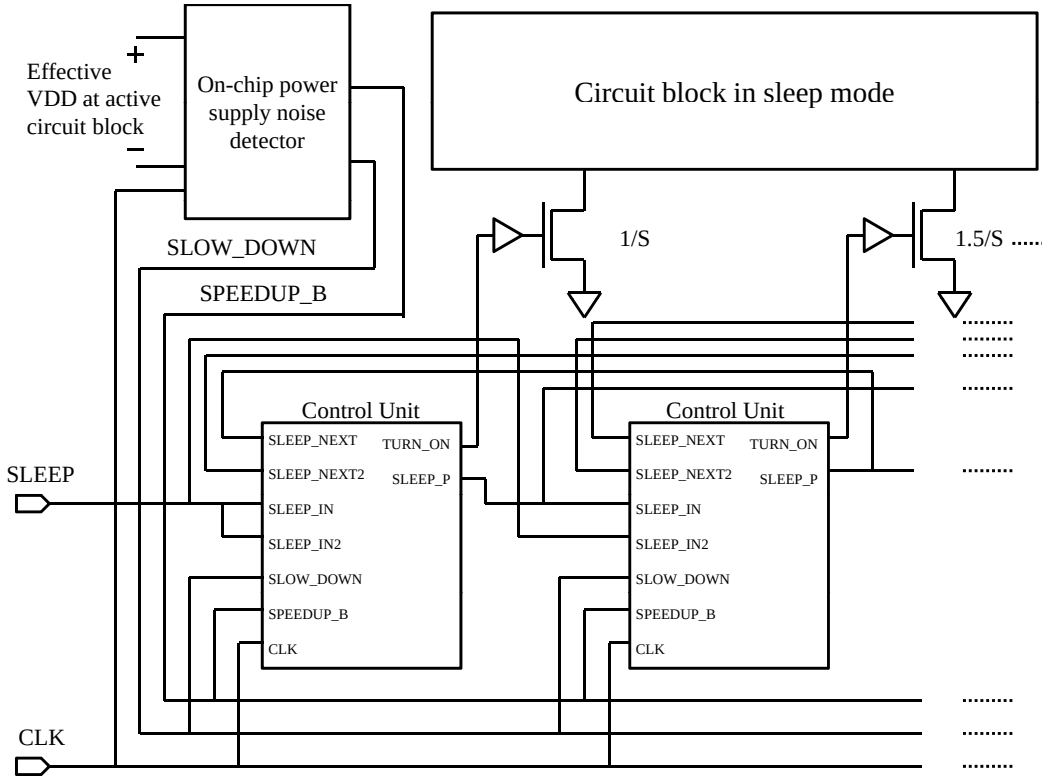


Figure 6.7: Circuit architecture of the dynamic reactivation throttling scheme

pre-determined threshold and de-asserts a SPEEDUP_B signal when it detects a low voltage drop. Though footer cells are used as the sleep transistors in this dynamic wakeup scheme, using header cells as the sleep transistors is also feasible. Only the polarity of the control signal needs to be changed if header cells are used.

As shown in Figure 6.7, the throttling control logic is inserted within each stage. The input of the control unit are the propagated SLEEP signals from the previous two stages and the next two stages (SLEEP_IN, SLEEP_IN2, SLEEP_NEXT, and SLEEP_NEXT2) as well as the SLOW_DOWN and SPEEDUP_B (active low)

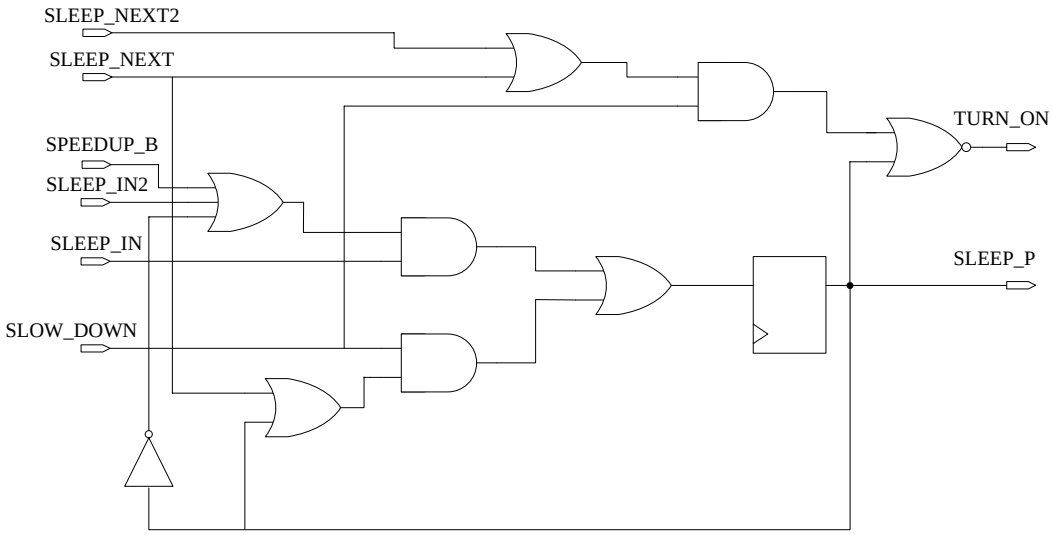


Figure 6.8: Control unit of the dynamic wakeup throttling scheme

signals from the on-chip detector. When the reactivation is executed, the SLEEP signal is de-asserted. The throttling control logic controls the propagation of the de-asserted SLEEP signal as illustrated in Figure 6.8.

The control unit follows the original wakeup sequence and propagates the de-asserted SLEEP signal one stage per clock cycle while the SLOW_DOWN signal is de-asserted and the SPEEDUP_B signal is asserted. When the SLOW_DOWN signal is asserted by the on-chip detector, the wakeup sequence will be rolled back for one stage. When both the SPEEDUP_B signal and the SLOW_DOWN are de-asserted, the de-asserted SLEEP signal will propagate two stages per clock cycle.

The output of the wakeup control unit contains the propagated SLEEP signal (SLEEP_P) and the TURN_ON signal. The SLEEP_P signal is the output signal connecting the next control unit stage and the TURN_ON signal controls the

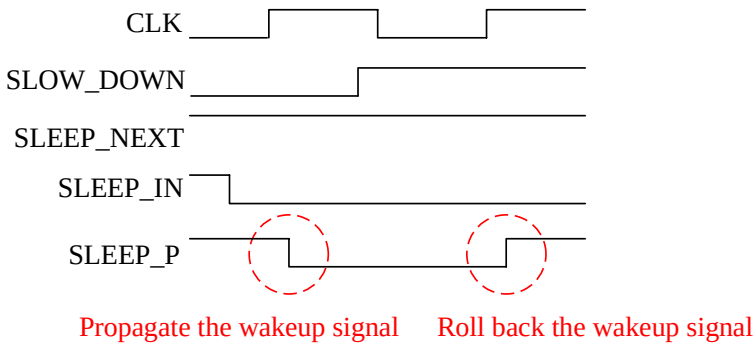


Figure 6.9: The operation of the SLEEP_P signal according to the SLOW_DOWN signal

ON/OFF of the footer cell. The SLEEP_P signal is controlled by the SLOW_DOWN and the SPEEDUP_B signals generated by the on-chip detector, and the SLEEP_IN and the SLEEP_IN2 signals generated from previous stages, and the SLEEP_NEXT signal from the next stage. The operation of the SLEEP_P signal is illustrated in Figure 6.9 and Figure 6.10.

In the ideal case, the SLOW_DOWN and the SPEEDUP_B signals should not be enabled at the same time. They should either be both disabled, or only one of them is enabled. If a detection error occurs causing the situation that the SPEEDUP_B signal is de-asserted and the SLOW_DOWN signal is asserted, the control unit will still roll back the wakeup sequence to prevent the excessive voltage drop. In this case, the wakeup signal does not move forward until the SLOW_DOWN signal is de-asserted.

The TURN_ON signal is controlled by the SLOW_DOWN signal, the SLEEP_P signals in current stage, and the SLEEP_P signals in the next two stages (SLEEP_NEXT

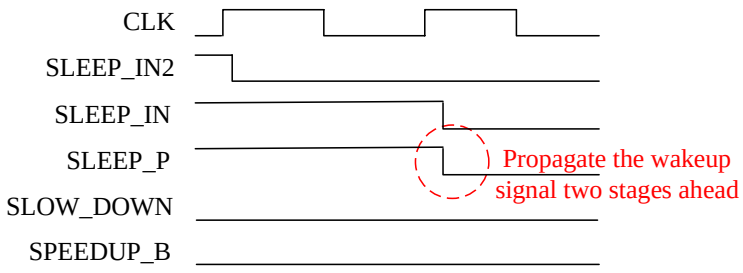


Figure 6.10: The operation of the SLEEP_P signal when propagating two stages in one cycle

and SLEEP_NEXT2). The TURN_ON signal will be asserted only when both the SLOW_DOWN signal and the SLEEP_P in the current stage are de-asserted, or when the SLOW_DOWN signal is asserted, but all of the three signals, SLEEP_P, SLEEP_NEXT, and SLEEP_NEXT2, are de-asserted. The operation of TURN_ON signal is illustrated in Figure 6.11.

The reason to use two individual signals as the output is to achieve more dynamic control on the wakeup sequence. The propagated wakeup signal SLEEP_P signal is updated once per cycle at the clock edge, which is not fast enough to take the immediate action. If the high ΔV_{active} is detected, the TURN_ON signal is able to make a faster response to reduce the rush current and avoid the high ΔV_{wakeup}. The reason to consider the SLEEP_NEXT and SLEEP_NEXT2 signal for the TURN_ON signal is to disable the TURN_ON signals in the recent three stages when the SLOW_DOWN signal is asserted.

By taking this approach, the ΔV_{wakeup} can be dynamically constrained according to the real-time ΔV_{active}, and extra voltage margin is created to accommo-

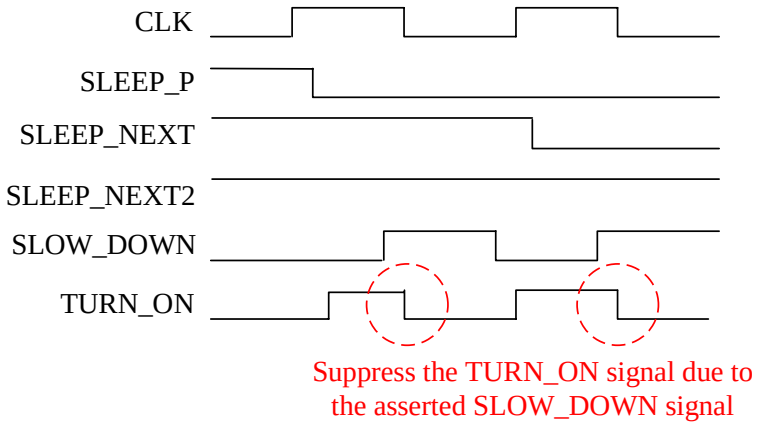


Figure 6.11: The operation of the TURN_ON signal

date the excessive ΔV_{active}. This approach efficiently solves the problem illustrated in Figure 6.3 without increasing significant fixed design cost. Also, the pessimism within the dynamic throttling scheme can be reduced.

6.3 Modifications to the SCOUT circuit

The on-chip detector used within this dynamic wakeup scheme is a simplified version of the SCOUT circuit, which is introduced in the previous chapter. Since this wakeup scheme needs to operate in real time with other active circuitry in normal operation mode, dynamic calibration of the detector is not allowed to characterize the on-chip detector. Therefore, the SCOUT circuit is the perfect candidate in this wakeup scheme, since the SCOUT circuit is robust against the process and temperature variation as discussed in the previous chapter. Moreover, the dynamic wakeup scheme would also benefit from the fast response time of the SCOUT cir-

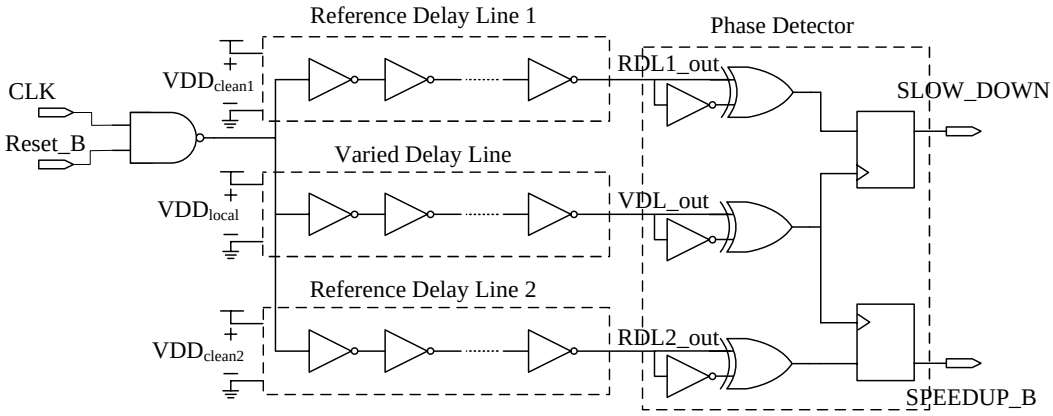


Figure 6.12: On-chip power supply noise detector implementation

cuit to provide an immediate alert signal before the circuit fails. Since only simple overshoot and undershoot for the SLOW_DOWN and SPEEDUP_B signals are required in this application, some modification is required on the original SCOUT circuit.

The simplified SCOUT circuit is illustrated in Figure 6.12. It is still composed of three parts, a voltage detector, a phase detector, and a reference voltage generator (not shown). The voltage generator provides two constant voltage sources regardless of the variations of the power supply, temperature, or the process. The voltage generator in the simplified version is the same as the original SCOUT circuit but with some modifications to the low-drop-out voltage regulator (LDO) to provide a different reference voltage level. Also, since two reference voltage sources are required in this wakeup scheme, the LDO needs to be duplicated to provide the second reference voltage source. However, the bandgap reference can be shared by the two LDOs, so single bandgap reference is sufficient.

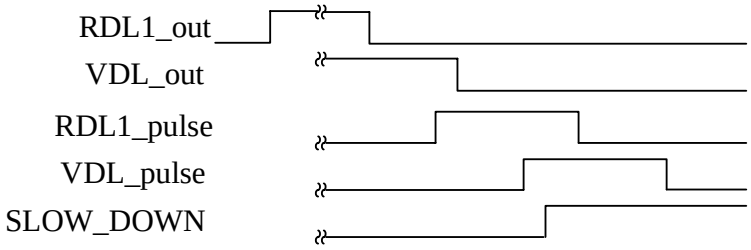


Figure 6.13: Timing diagram of the power supply noise detector

There is also some minor modification to the voltage detector in the simplified version from the original SCOUT circuit. The voltage detector in the simplified version contains three identical delay lines, two reference delay lines (RDL1 and RDL2) and one varied delay line (VDL). The RDL1 and RDL2 are supplied by the two reference voltage sources respectively, which are provided by the reference voltage generator. Both the outputs of the two RDLs connect to two phase detectors. All of the three delay lines are triggered by the clock signal. Therefore, the SCOUT circuit can update the status of supply noise twice per cycle. In addition, the small inverter, INV_{tail}, following the $INV_{regular}$ in the original SCOUT circuit is removed in the simplified version. The original purpose of the INV_{tail} is to achieve a homogeneous implementation between the voltage detector and the phase detector. However, this requirement is not needed in this application.

The major modification to this simplified version is the implementation of the phase detector. The phase detector contains only three pulse generators and two flip-flops to capture the phase difference between the RDL1_out and VDL_out signals and between the RDL2_out and the VDL_out signals. When the voltage differ-

ence between the two reference voltage and the VDD_{local} exceeds a pre-determined threshold, the SLOW_DOWN signal or the SPEEDUP_B signal will be triggered as illustrated in Figure 6.13. The original SCOUT circuit generates the detection results in an absolute value. Therefore, the original phase detector needs to be implemented in a homogeneous manner as the voltage detector. However, a single undershoot/overshoot detection result is sufficient for the purpose of providing the real-time alert to the wakeup scheme.

6.4 Advantage and limitation

One advantage of this dynamic throttling scheme is the flexibility to accommodate any situation after the chip is fabricated. Therefore, this scheme is able to be adjusted according to the needs after the chip is fabricated. For example, the speed up and slow down mechanism can be adjusted by tuning the reference voltage generated by the LDOs. Also, this dynamic throttling scheme is still be able to perform the conventional wakeup by simply masking the SLOW_DOWN and the SPEEDUP_B signals with basic logic gates. For example, the voltage margin may be big enough to cover the absolute maximum value of $\Delta V_{active} + \Delta V_{wakeup}$ after the post fabrication characterization. In this case, the slow down mechanism can be disabled and the wakeup throttling scheme will not lose any wakeup efficiency. Or, if robustness is the only concern and wakeup time is not an issue, the speedup mechanism can be disabled to guarantee a slow pace of the wakeup signal propagation.

There is one limitation for this dynamic wakeup scheme, which is the varia-

tions of the voltage thresholds of the SLOW_DOWN and the SPEEDUP_B signals. This variation originates mainly from the temperature variation acting upon the bandgap reference. Therefore, the $\Delta V_{tolerable}$ may not be able to be constrained exactly the same as the desired value within this dynamic wakeup scheme. As a result, some extra pessimism is required to cover this variation. In some circumstances, the wakeup sequence would be held, even though it may not be required. However, the speed up mechanism is able to compensate the loss of wakeup efficiency. Therefore, this scheme is still competitive, compared with other approaches illustrated in Figure 6.4, which require fixed design costs.

To solve the problem of the variation of the voltage threshold of the SLOW_DOWN and SPEEDUP_B signals, the reference voltage generator can be replaced by other temperature-insensitive and stable voltage sources. It can utilize dedicated power pins or design a less temperature sensitive bandgap reference. However, optimizing the bandgap reference is out of the major scope of this wakeup scheme, so it will not be discussed here.

Another drawback within the dynamic wakeup throttling scheme is that the wakeup time may vary according to the ambient voltage level. Therefore, some extra work will be required on the operating system side and the software side to accommodate the varying wakeup time.

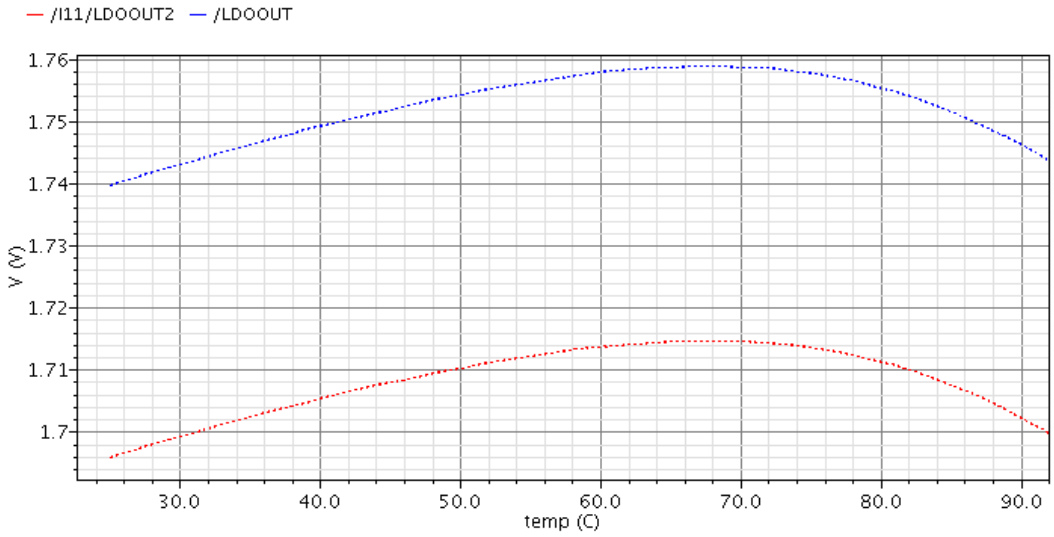


Figure 6.14: Reference voltage for two RDLs respect to temperature variation

6.5 Implementation and simulation results of the power supply noise detector

The simplified SCOUT circuit is implemented in the TSMC 0.18μm technology (typical VDD = 1.8V). Both the RDLs and VDL consist of 42 inverters. For the purpose of reducing the simulation time while verifying the dynamic wakeup throttling, the reference voltage generator is replaced by a DC voltage source during simulation. Therefore, the generator needs to be characterized first. The major source varying the reference voltage is the temperature variation acting upon the bandgap reference. We assume that the operating temperature of the circuit ranges between 25 °C and 90 °C, VDD_{clean1} varies between 1.696V and 1.715V, and VDD_{clean2} varies between 1.740V and 1.759V as shown by Spectre simulation in Figure 6.14.

Table 6.1: Voltage threshold for the SLOW_DOWN signal at fifteen combinations of corners {FF, FNSP, SNFP, SS, and TT} and temperatures {25 °C, 66 °C, and 90 °C}

	FF	FNSP	SNFP	SS	TT
25 °C	1.694V	1.695V	1.692V	1.692V	1.693V
66 °C	1.712V	1.711V	1.709V	1.711V	1.711V
90 °C	1.697V	1.700V	1.698V	1.697V	1.698V

The detector is designed with a voltage threshold for the SLOW_DOWN and SPEEDUP_B signals of approximately 1.702V and 1.745 respectively. Corner-based simulations were performed on the detector to characterize the detection results and to find out the maximum possible error in those extreme corners. The simulation was performed on the pre-layout netlist with HSPICE. The detector is simulated at fifteen different combinations of five processes (FF, FNSP, SNFP, SS, and TT) and three temperatures (25 °C, 66 °C, and 90 °C). The DC value of the reference voltage is assigned according to different temperatures as shown in Figure 6.14. The local VDD sweeps slowly and linearly across a range, 1.8±0.15V.

The voltage thresholds of the SLOW_DOWN and SPEEDUP_B signals for these fifteen corners are listed in Table 6.1 and Table 6.2. Simulation results show that the voltage thresholds for the SLOW_DOWN and the SPEEDUP_B signals range between 1.702±0.011V and 1.746±0.010V respectively within the 15 corners without any calibration. The time resolution for the fifteen corners is listed in Table 6.3, which ranges between 1.285±0.255ns.

Table 6.2: Voltage threshold for the SPEEDUP_B signal at fifteen combinations of corners {FF, FNSP, SNFP, SS, and TT} and temperatures {25 °C, 66 °C, and 90 °C}

	FF	FNSP	SNFP	SS	TT
25 °C	1.737V	1.739V	1.737V	1.738V	1.738V
66 °C	1.754V	1.756V	1.752V	1.753V	1.755V
90 °C	1.739V	1.739V	1.737V	1.737V	1.740V

Table 6.3: Time resolution of the detectable noise at fifteen combinations of corners {FF, FNSP, SNFP, SS, and TT} and temperatures {25 °C, 66 °C, and 90 °C}

	FF	FNSP	SNFP	SS	TT
25 °C	1.03ns	1.22ns	1.20ns	1.42ns	1.20ns
66 °C	1.08ns	1.29ns	1.27ns	1.48ns	1.28ns
90 °C	1.10ns	1.34ns	1.30ns	1.56ns	1.34ns

6.6 Implementation and simulation results of the dynamic wakeup throttling

6.6.1 Experiment setup

The circuit block to be woken up in the experiment contains two high speed Fast Fourier Transform cores with footers as the power gating cells. The FFT circuit is also implemented in the TSMC 0.18μm technology with a 400MHz clock. The dimension of the FFT block is 1260$\mu m \times 1260\mu m$, which occupies 1/9 of the total area (3780$\mu m \times 37800\mu m$) and sits in the middle of the chip as shown in Figure 6.15. This experiment setup models the worst possible case for a wire-bond

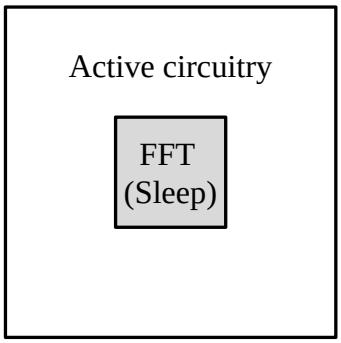


Figure 6.15: The circuit model for the experiment

package design. There are a total of 24 power pins for VDD and VSS in the test circuit implementation.

In order to simulate the power supply noise for the whole chip, an equivalent RLC model similar to [62] was built as shown in Figure 6.16. Assume the active circuitry has a current consumption similar to the FFT block. The current density function, $J(t)$, of the active circuitry is modeled from the current waveform of the FFT. The average current waveform (vectorless) of the FFT block is first extracted with Primetime PX. This current waveform can be modeled as a piece-wise-linear model to ease the current modeling in simulation as shown in Figure 6.17. Based on this PWL current waveform, the current density function, $J(t)$, can be calculated to model the circuit activity of the active circuitry. $J(t)$ is multiplied by a factor k to model the level of activity. When $k < 1$, the activity of the active circuitry is lower than average; when $k > 1$, the activity of the active circuitry is higher than average. In the following experiment, it is assumed that the estimated maximum voltage drop happens when $k = 1.5$. The maximum factor k for unpredicted high activity should

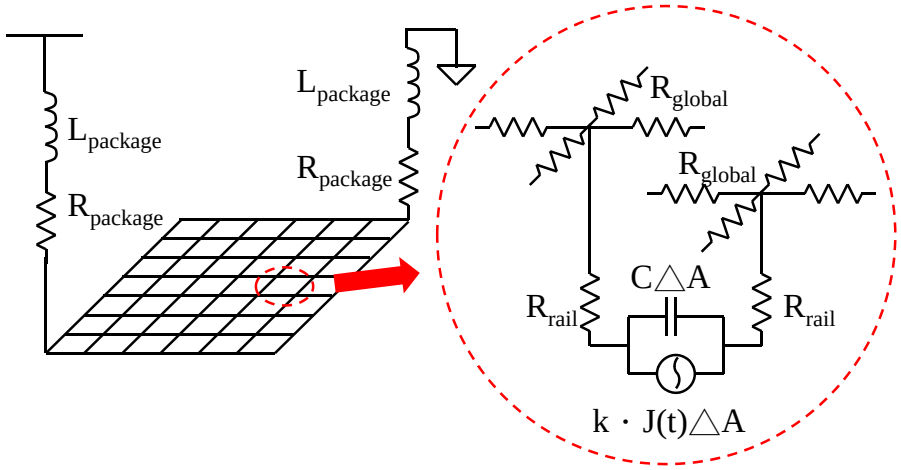


Figure 6.16: RLC model for power distribution network

not exceed 2.25 for a reasonable experiment. This is because simulation results show that the ΔV_{active} induced by the active circuitry is 130mV when k is a constant 2.25 without reactivating the sleeping blocks. Therefore, if the factor k exceeds 2.25, the robustness of the wakeup scheme cannot be evaluated, since a voltage drop violation always occurs. Regarding the RC model of the FFT block, there is not a current source for the FFT block, since it is in sleep mode. The virtual VSS net is assumed to be charged to VDD by a pull-up PMOS as in [63] for simulating the worst-case wakeup time.

6.6.2 Reactivate under extreme cases using conventional wakeup scheme

The conventional wakeup scheme is first evaluated under extreme cases to identify the required design resources to cover the unpredicted high ΔV_{active}. To identify the maximum voltage drop when the ΔV_{active} is within the estimated range,

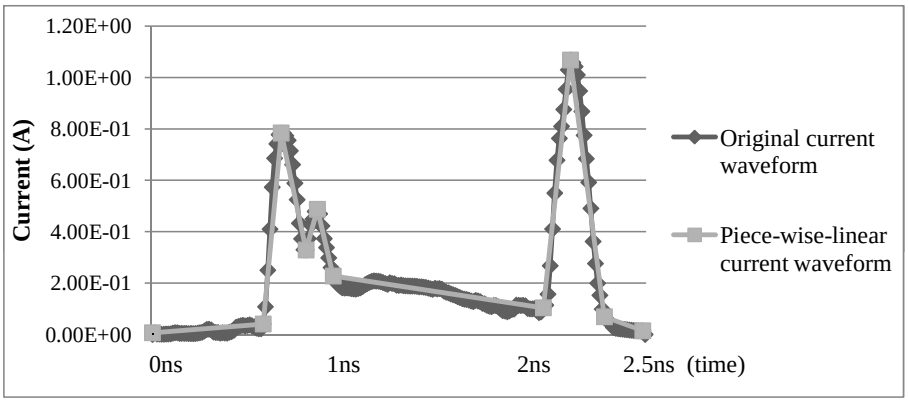


Figure 6.17: Piece-wise-linear current model for the active circuitry within one clock cycle

Table 6.4: Maximum voltage drop when the sleeping block is reactivated under high ΔV_{active}

Circuit activity	$k = 1.5$	$k = 2.0$
Maximum voltage drop	130mV	157mV

the conventional scheme is simulated with a constant k factor 1.5 during wakeup. It is also simulated if the active circuitry generates an unpredicted high voltage drop. The maximum unpredicted high activity is assumed to be $k = 2.0$ in this experiment to maintain some margin for the ΔV_{wakeup}. The simulation results are listed in Table 6.4.

From Table 6.4, the maximum voltage drop increases 27mV when the sleeping block is reactivated under unpredicted high ΔV_{active} using the conventional scheme. The wakeup time is 35ns. If raising VDD and widening the power net-

Table 6.5: The maximum voltage drop with extended wakeup time in the conventional scheme

Sizing ratio of footers	Maximum voltage drop	Wakeup time	
×1.5	157mV	35ns	100%
×1.4	152mV	37.5ns	107%
×1.3	144mV	40ns	114%
×1.2	138mV	42.5ns	121%
×1.15	134mV	47.5ns	136%

work are not allowed, the wakeup time of the conventional wakeup scheme needs to be extended. To identify this required extended wakeup time, the conventional wakeup scheme is modified with longer wakeup time and the simulation results are listed in Table 6.5.

From the simulation results, if we use the first method in Figure 6.4 to cover the unpredicted high ΔV_{active} when k is up to 2.0, VDD needs to be raised for 27mV (+21% voltage margin from 130mV). This design cost may become even more significant if a lower VDD is used in advanced technologies. If we use the seconde method in Figure 6.4, we also need to increase roughly +21% wire width of the original power network. As power network typically occupies more than 15% of area in each metal layer, this increase of power net width is significant. If we use the third method in Figure 6.4, the wakeup time need to be permanently extended more than +36% of original wakeup time. Therefore, either method requires considerable fixed design cost.

6.6.3 Reactivate under random activity

To validate robustness and wakeup efficiency of the dynamic wakeup scheme, Monte Carlo simulation is performed considering different levels of the ΔV_{active} with HSPICE. The random circuit activity of the surrounding active circuitry is generated by assigning the factor k through a random number generator. The random number k is constrained within the given range according to the activity level of interest. To consider the impact of the intra-die process variation on the on-chip detector, the netlist utilizes the static model with different seeds for each test case. The random intra-die process variation is introduced by inserting random Vt variation into each individual transistor within the on-chip detector. The random Vt variation spans $\pm 2\sigma$ of the standard deviation on top of the inter-die variation. The temperature is randomly assigned between 25 °C to 90 °C. The DC value of the reference voltage depends on the simulation temperature and is assigned according to Figure 6.14.

6.6.3.1 Reactivate under high ΔV_{active}

To evaluate robustness of the dynamic wakeup throttling scheme, the conventional wakeup scheme and the dynamic wakeup scheme are simulated when the active circuitry generates a high ΔV_{active}. The random number uniformly ranges from 0.75 to 2.0 and total 2500 random test cases are simulated. The distribution of maximum voltage drop is illustrated in Figure 6.18

From Figure 6.18, voltage drop violations occur in 806 test cases for the conventional wakeup scheme, while there are only 21 violations for the dynamic

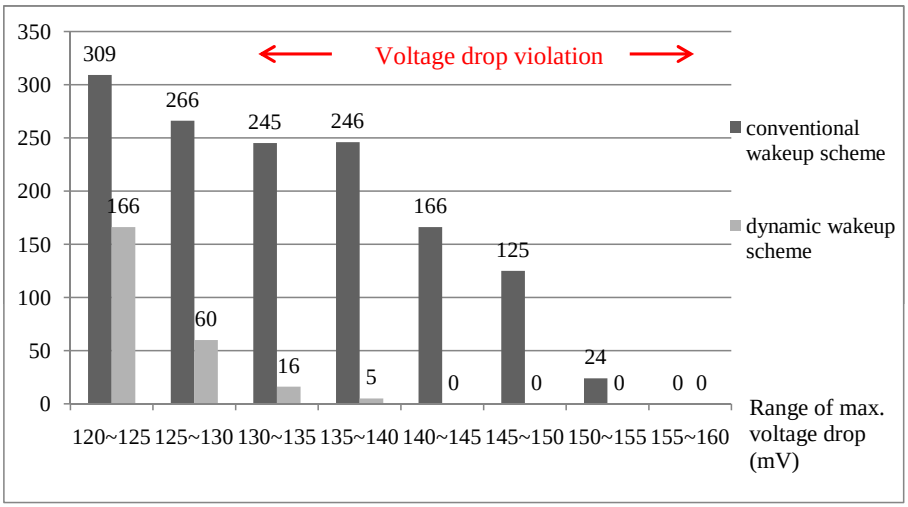


Figure 6.18: Distribution of maximum voltage drop within 2500 random test cases

wakeup scheme. Therefore, the dynamic wakeup scheme is able to reduce the possibility of voltage drop violation 97.4% compared with the conventional scheme. In addition, the magnitude of violation also reduces significantly. Hence, the chance of circuit failure resulted from these violations also reduces.

The maximum voltage drop and the average wakeup time for both schemes are summarized in Table 6.6. It can be noted that the average wakeup time increases significantly for the dynamic wakeup scheme. This is because this experiment considers the circuit activity much higher than average case. It does not reflect the wakeup efficiency in general cases. However, this result reveals that the estimation of the ΔV_{active} can not be overly optimistic even with the dynamic wakeup throttling. Although the maximum voltage drop is still under constraint, the increasing wakeup time may become un-affordable.

Table 6.6: Reactivate the FFT block under high ΔV_{active} ($0.75 < k < 2.0$) for both schemes

	Conventional wakeup scheme		With dynamic wakeup throttling	
Average wakeup time	35.0ns	100%	76.0ns	217%
Maximum voltage drop	154mV	100%	137mV	89%

6.6.3.2 Reactivate the FFT block under average ΔV_{active}

Wakeup efficiency of the dynamic wakeup scheme is evaluated when the surrounding active circuitry introduces an average ΔV_{active}. Both wakeup schemes are simulated when the parameter k uniformly ranges from 0.5 to 1.5 for 1000 random test cases. The maximum voltage drop and the average wakeup time for both scheme are summarized in Table 6.7. It can be found that the average wakeup time for the dynamic wakeup scheme is only +2% longer compared with the time for the conventional wakeup scheme. Therefore, the loss of wakeup efficiency is very small when ΔV_{active} is within the estimated range. Also, the average power consumption during wakeup for the dynamic wakeup scheme is 3.46W, and the average power consumption for the conventional wakeup scheme is 3.41W. Therefore, the dynamic wakeup scheme does not contribute to significant power consumption.

Table 6.7: Reactivate the power gating under average ΔV_{active} ($0.5 < k < 1.5$) with and without the dynamic wakeup sequence throttling

	Conventional wakeup scheme		With dynamic wakeup throttling	
Average wakeup time	35.0ns	100%	35.7ns	102%
Maximum voltage drop	126mV	100%	125mV	99%

6.6.3.3 Reactivate during a wide range of ΔV_{active}

To evaluate robustness and wakeup efficiency of the dynamic wakeup scheme in a more general case, both of the two schemes are simulated with a wide range of the parameter k, which ranges from 0.25 to 2.0. Since the extreme ΔV_{active} should not occur frequently in a proper design, a random value of k is generated with a normal distribution random number generator with the average 1.0 and the standard deviation 0.5. The value for k is discarded if it exceeds the range of interest. Therefore, the possibility of extreme ΔV_{active} is lower than the possibility of average ΔV_{active}. The distribution of maximum voltage drop within 2000 random test cases is illustrated in Figure 6.19. The possibility of a voltage drop violation in the dynamic wakeup scheme also reduces significantly compared with the conventional wakeup scheme.

The maximum voltage drop and average wakeup time are summarized in Table 6.8. The average wakeup time of the dynamic wakeup throttling scheme becomes closer to the average case while the maximum voltage drop is much lower than the maximum voltage drop when using the conventional scheme. The average

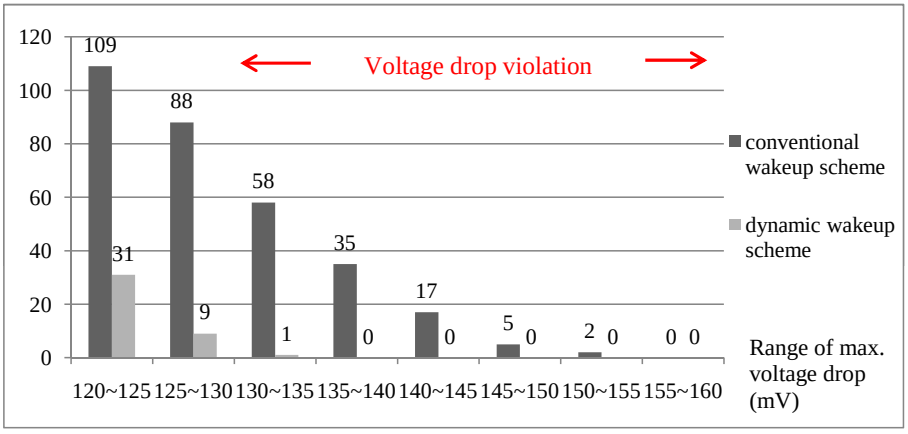


Figure 6.19: Distribution of maximum voltage drop within 2000 random test cases when $0.25 < k < 2.0$

Table 6.8: Reactivate the FFT block under a wide range of ΔV_{active} ($0.25 < k < 2.0$) for both wakeup schemes

	Conventional wakeup scheme		With dynamic wakeup throttling	
Average wakeup time	35.0ns	100%	39.7ns	113%
Maximum voltage drop	151mV	100%	131mV	87%

wakeup time of the dynamic wakeup scheme is still slightly higher compared with the wakeup time in Table 6.7 because of the occurrence of unpredicted high ΔV_{active} in this experiment.

Table 6.9: Reactivate the FFT block under low ΔV_{active} ($0.25 < k < 1.25$) for both schemes

	Conventional wakeup scheme		With dynamic wakeup throttling	
Average wakeup time	35.0ns	100%	27.1ns	77.4%
Maximum voltage drop	113mV	100%	111mV	98%

6.6.3.4 Reactivate under low ΔV_{active}

This experiment considers the case if the ΔV_{active} is over-estimated that the actual circuit activity level is lower than the estimated value. Therefore, the two wakeup schemes are simulated when the ΔV_{active} is in a lower range ($0.25 < k < 1.25$). The simulation results of 500 random test cases are summarized in Table 6.9. Table 6.9 shows that the dynamic wakeup scheme is able to reduce 22.6% of the wakeup time on average compared with the conventional scheme. This result indicates that the dynamic wakeup scheme is able to gain efficiency back by reducing the wakeup time when the ΔV_{active} is over-estimated. Therefore, fewer design resources are wasted compared with the conventional wakeup scheme which takes a fixed wakeup sequence.

6.6.4 Sensitivity analysis between maximum voltage drop and random factor k within the dynamic wakeup scheme

To analyze the impact of different high ΔV_{active} to both wakeup schemes, this experiment compares the maximum voltage drop when differen level of unpredicted high ΔV_{active} occur. Both wakeup schemes are verified when the level of activity ranging from $0.75 < k < 1.75$ to $0.75 < k < 2.25$. The distribution of maximum voltage drop within 2000 random test cases when $0.75 < k < 1.75$ and $0.75 < k < 2.25$ is illustrated in Figure 6.20 and Figure 6.21. The possibility of the occurrence of voltage drop violation of two wakeup schemes with different k ranges is summarized in Figure 6.22. From Figure 6.22, the possibility increases significantly with the increase in k while using the conventional wakeup scheme. On the contrary, the possibility increases only slightly with the increase in k while using the dynamic wakeup scheme. Therefore, it can be concluded that the dynamic wakeup scheme is less sensitive to the unpredicted high ΔV_{active} compared with the conventional wakeup scheme.

6.7 Summary

This chapter presents a new power gating reactivation scheme to dynamically throttle the wakeup sequence for power gating techniques. This wakeup scheme is robust against excessive voltage drop due to an unpredicted high activity during the wakeup phase. By utilizing a SCOUT detector, the wakeup scheme is aware of the real-time voltage drop and is able to throttle the wakeup sequence when a high voltage drop is detected and to speed up the wakeup sequence when

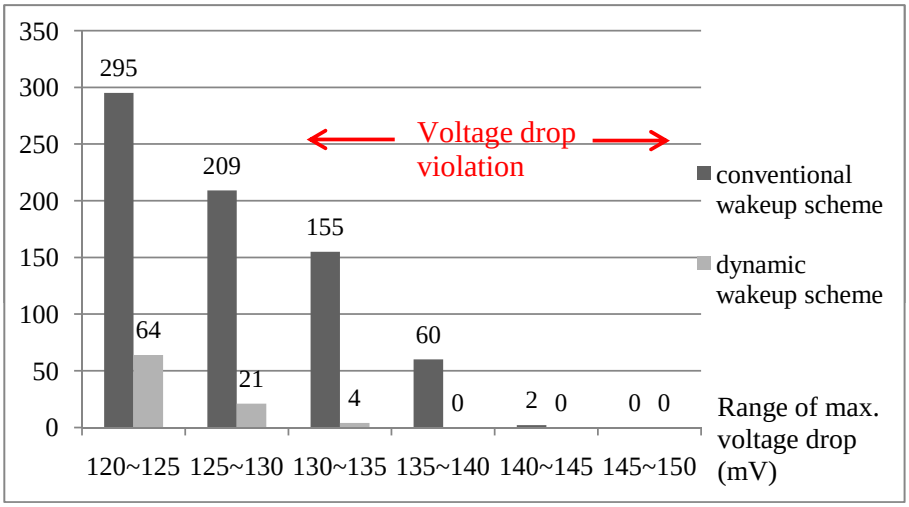


Figure 6.20: Distribution of maximum voltage drop within 2000 random test cases when $0.75 < k < 1.75$

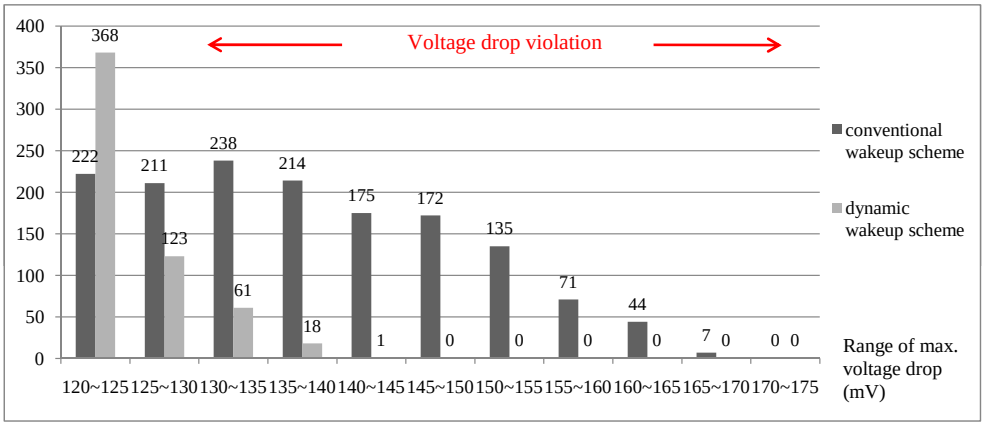


Figure 6.21: Distribution of maximum voltage drop within 2000 random test cases when $0.75 < k < 2.25$

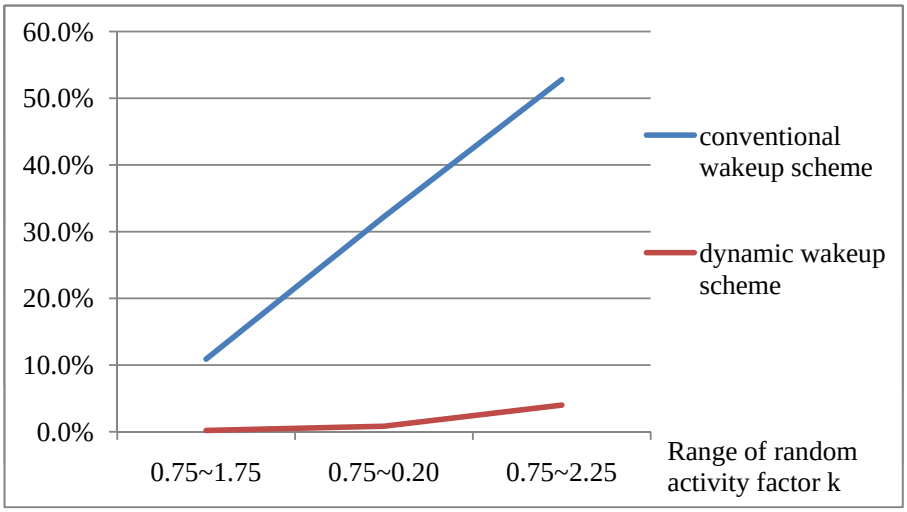


Figure 6.22: Possibility of the occurrence of voltage drop violation when random k series is within different ranges

a low voltage drop is detected. The simulation results show that this technique is able to effectively constrain the ΔV_{wakeup} according to the ΔV_{active} in real time. In addition, the maximum voltage drop during power gating reactivation becomes less sensitive while using the dynamic wakeup scheme compared with using the conventional wakeup scheme. Even the adjacent active circuit blocks induce an unexpectedly high voltage drop, the possibility of the occurrence of excessive voltage drop is reduced significantly, without adding fixed design cost, such as raising the VDD level, increasing the decap, widening the power network, or permanently prolonging the wakeup time. Moreover, this dynamic wakeup scheme is also able to improve the wakeup efficiency when the ΔV_{active} is lower than the estimated value. Hence, it can achieve more efficient design resource usage.

Chapter 7

Conclusion and future direction

This dissertation presents designs and design methodologies that manage the issues resulting from power supply noise during different design phases. These designs and techniques improve current available techniques and tackle the problem resulting from power supply noise in more effective and efficient ways. As power supply noise becomes a more critical issue in current and future technologies, more research efforts should be devoted in this field.

7.1 Power supply noise estimation

A systematic methodology to search the circuit activity effectively and efficiently is presented in Chapter 3. This methodology comprehensively covers all essential factors in the cost function formulation. These factors comprise the physical implementation, power consumption, current waveform, and circuit functionality. As a result, the impact of the circuit activity on the power supply noise can be more accurately reflected.

This methodology also uses powerful search tool and hierarchical validation method. Therefore, the estimated power supply noise reflects a realistic estimation. Following this methodology, designers are able to be aware of the power supply

noise issues and enhance the power distribution in the light of the estimation results. Hence, the path slow-down issue caused by voltage drop can be predicted and avoided, and thus the design quality can be improved.

However, some issues in the supply noise estimation techniques remain to be solved. For example, current existing techniques can only estimate a lower bound or a loose upper bound rather than a tight and reasonable upper bound. Notwithstanding, estimation of a tight and reasonable upper bound plays a significant role for design quality and deserves more research effort in the future.

Another unsolved issue is to improve the quality of vectorless estimation. As discussed previously, finding the circuit activity inducing the maximum voltage is the most difficult challenge while estimating power supply noise. The vectorless estimation is able to significantly save design resources and time when compared to finding a specific circuit activity. However, the current vectorless estimation methodology utilizes a probability approach and considers factors only at the circuit level. As a result, it is difficult to describe the circuit behavior and to estimate the mid-frequency supply noise. Migrating the vectorless estimation up to either the architecture level or the application level will dramatically improve the estimation quality. Improving the current vectorless estimation methodology will be a valuable investment.

7.2 Power supply noise detection

Two different on-chip power supply noise detectors are presented in Chapter 4 and Chapter 5 respectively, which improve the visibility of voltage drop during

test phase. This visibility can help the designer to understand why the path slows down or why the circuit fails. It is also able to provide precious feedback on improving the design flow and avoiding the same problem occurring in the future projects.

The first on-chip detector presented in Chapter 4 is capable of reducing the area consumption of the detector when there are numerous detection locations of interest. This detector utilizes ring oscillator to monitor the local VDD value and a dedicated divider to evaluate the detection results. Area saving is achieved by sharing the common part of each detector as much as possible. Hence, the design cost of the on-chip detector can be significantly reduced. If 64 detectors is embedded into a chip, the area consumption is able to reduce more than 15 times smaller compared with a conventional design. In addition, the simulation result shows that there is no accuracy lost while the area is significantly reduced. This purely digital scheme can be inserted into any design as a hard macro to reduce the design complexity.

The second on-chip detector presented in Chapter 5 utilizes a voltage detector to detect the voltage difference between the local VDD and the reference voltage source and generates two signals with a phase difference. The phase difference is detected by a phase detector with a homogeneous implementation as the voltage detector. This detector meets most of the expectations of an on-chip power supply noise detector. First, this detector performs self-calibration and provides accurate result in any circumstance. Second, the detector is able to continuously monitor power supply noise and does not miss any information between measure-

ments. Third, the detector generates the detected results in an absolute value rather than a simple overshoot or undershoot. With these characteristics, this detector proves to be the best candidate to provide a real-time alert. Also, it can provide more comprehensive information for debugging purposes.

7.3 Power supply noise reduction

A novel dynamic power gating reactivation scheme is presented in Chapter 6. This scheme utilizes the on-chip detector presented in Chapter 5 to monitor power supply noise in real time. It takes a dynamic approach controlling the wakeup sequence according to the ambient voltage level. The wakeup sequence is throttled when the detector detects a high voltage drop, and the wakeup sequence is speeded up when a low voltage drop is detected. Hence, the voltage drop caused by the rush current can be constrained immediately. The simulation results have demonstrated the ability to prevent an excessive voltage drop when the ambient active circuitry induces a high voltage drop during the wakeup phase. Simulation results show that the dynamic wakeup scheme is able to reduce the possibility of voltage drop violation 97.4% compared with the conventional scheme when a ΔV_{active} occurs. As a result, the fixed design resource, which is used to prevent the voltage emergency, can potentially be reduced by utilizing this dynamic reactivation scheme. Moreover, this dynamic wakeup scheme is also able to improve the wakeup efficiency when the ΔV_{active} is lower than the estimated value. Hence, this dynamic wakeup scheme can achieve more efficient design resource usage.

Nowadays, designers design circuits with more delicate techniques and try

every method to reduce design margin for the purpose of saving power, saving energy, and improving performance. It is obvious that if the behavior of chips, such as the clock frequency, supply voltage, or the wakeup sequence of the power gating reactivation, is fixed, more or less there is a loss of efficiency for the design resources usage. Using on-chip detector in a chip is able to characterize the circuit in the field, and real-time tuning during normal operation in response to process and environmental variability becomes possible. An example for this type of on-line tuning strategy is the real-time power management within the IBM POWER6 processor [64]. Another example is the dynamic power gating reactivation scheme presented in the previous chapter. Future opportunities should exist for using the on-chip detector to actively improve the design quality.

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